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ADVISORY GROUP FOR AEROSPACE RESEARCH & DEVELOPMENT
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AGARDograph 329

Applications of ASICs to Avionics

(Applications des ASICs dans les Equipements Avioniques)

This AGARDograph was sponsored by the Avionics Panel of AGARD.

NORTH ATLANTIC TREATY ORGANIZATION

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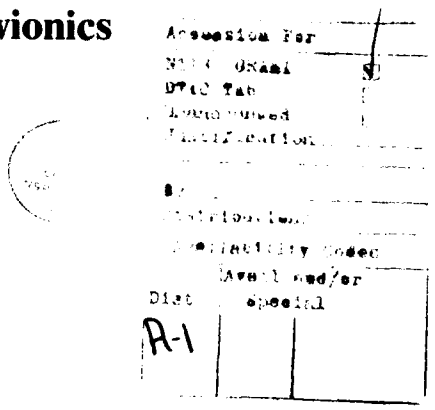

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Preface

This AGARDograph dedicated to ASICs (Application Specific Integrated Circuits) is aimed at providing the non specialists of IC design with an overview of the technical features of such circuits, the technologies and development methods used for their realization.

After a summary of the basic principles of the ASIC approach, the state of the art of products and their evolution, several practical applications are presented by users, in the avionics area in particular.

It will be shown, through the successive chapters of this document, that the ASICs need three main supports: the technology, the CAD system and the digital or analog function library.

More than for the other integrated circuit categories, it is the conjunction of those three areas and their correlated advances which enable the realization of very high performance circuits, fulfilling the stringent requirements of avionics, in terms of complexity, weight, volume and operating speed.

The intelligence and the performance of military equipments, for avionics in particular, more and more lie with the silicon of the ASICs.

JM. Brice

Préface

Cette AGARDographie, consacré aux ASICs (Application Specific Integrated Circuits), est destiné à l'usage des non spécialistes qui désirent avoir une idée des possibilités techniques offertes par ces circuits, ainsi qu'une vue synthétique des technologies et méthodes de conception mises en oeuvre pour les réaliser.

Après un rappel des principes de base de l'approche ASIC, de l'état de l'art actuel des produits et de leur évolution, plusieurs applications pratiques sont rapportées par des utilisateurs, en particulier dans le domaine de l'avionique.

On verra à travers les divers chapitres de ce document que les ASICs reposent sur trois grands "piliers": la technologie, la CAO et les bibliothèques de fonctions logiques ou analogiques. Plus que pour les autres catégories de circuits électroniques intégrés, c'est la conjonction de ces trois domaines, et la cohérence de leurs progrès, qui permettent de réaliser des applications extrêmement performantes, qui satisfont en particulier les exigences sévères de l'avionique en matière de complexité, de poids, de volume et de vitesse.

Il n'est pas vain de dire que l'intelligence et les performances des équipements militaires et avioniques en particulier reposent sur le silicium des ASICs.

JM. Brice

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WHAT IS AN ASIC ?

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1. INTRODUCTION

Since the emergence of the first ASICs, in the 1975's, there has been a lot of advances in this field, leading to very high complexity digital ASICs or to very high speed analog circuits. But this strong evolution did not really change the nature of the ASIC families which are presently four : full custom circuits, standard cells, programmable devices and PLD's.

Before detailing these families with their characteristics, the principles and drawbacks of the ASIC approach have to be explained and some definitions have to be given.

2. ASIC PRINCIPLES

The ASIC acronym means Application Specific Integrated Circuit, which clearly indicates that these particular circuits are designed according to a given specification relating to a particular application. At the opposite, a standard circuit exhibits a fairly general specification fitting to many applications.

An ASIC is usable for only one application or one class of applications but its specification exactly matches these particular technical requirements, whereas a standard circuit has a general purpose specification, fitting to many different applications, but with trade-offs leading sometimes to degraded performances of the system.

As an example, a digital signal processor is a standard circuit allowing the user to realize fast Fourier Transform operations in particular, but also many other signal processing operations. For certain applications, requiring only a high performance FFT operator, it may be of interest to design a specific circuit, whose unique function will be to perform FFT's at very high speed, with input/output organisation fitting exactly to the application. Such a circuit will be an ASIC, executing only FFT's with high performances unlike the standard signal processor able to execute many processses, but each with moderate performances.

This simple example shows the primary interest of the ASICs : to exactly meet the specifications of the application, leading to a very good optimization of the size, complexity and cost of the complete system. But ASICs exhibit other advantages which will appear in the next chapters.

3. THE ASIC FAMILIES

There are 4 major types of ASICs, using two approaches ; one called "custom", the other called "semi-custom".

3.1 The custom approach

This technique consists in designing the circuit by using components tailored to meet the requirements of the specification.

The designer can work at the component level, including the possibility to create a new component, or at the cell level when standard functions can be used such as OP amplifier, flip-flop, etc...

3.1.1 *Full custom design*

When only basic components (transistors, resistors, capacitances) are used and tailored for the specific need of the circuit, the method of design is called "full custom".

CAD tools are used much like as in the case of standard circuit design : schematic editor, simulator, graphic editor...

This approach is mainly used for ASICs requiring very tight optimization of the functions, unachievable with standard functions and automatized CAD tools.

Such a circuit is tailored to the desired application and can be optimized in term of performance and silicon area, but the design effort and the lead time are comparable to the ones of standard circuits. In addition, it requires experienced designers, not always available in the equipments manufacturer environment. This is why this approach is used

only when there is no other more efficient way to realize the ASIC. An example of a full custom ASIC is given in figure 1.

Figure 1

3.1.2 *Standard cell design*
When the circuit can be achieved using a library of predefined functions such as basic gates, I/O buffers, macrocells (RAM, PLA, MPY, register file), OP amplifiers, regulors, PLL...., the method of design is called "standard cell".

This technique brings a high efficiency to the ASIC design and allows the user to benefit from powerful CAD tools available on the market. He does not have to go down to the component level but, instead, to handle functions made with cells.

Those cells and macrocells have been tested on silicon by the ASIC vendor during the development stage of the library so as to offer a set of functions which are fully validated and characterized in terms of behaviour and timing performances. In other words, those cells are "design error free" and their specifications have been controlled on silicon.

Thus, the ASIC designer can focus on the assembly of the cells necessary to his application, using CAD tools : schematic capture, simulator, place and route software, layout edition and testing.

The additional step of a standard cell circuit design is the placement operation, consisting of taking the cells selected for the circuit and abutting them to constitute rows separated by free space for interconnections. This placement can be automatic but has to be "designer assisted" to save space, get the best density and optimise dynamic aspects. To facilitate the placement and the routing of the cells, they are designed according to basic rules : defined height, width multiple of a grid pitch, terminals carefully placed on the sides of the cells, etc... This is why they are called "standard cells".

The rows of abutted cells are separated by channels used by the router software to interconnect the cells. Once the circuit is fully routed, a checking procedure takes place to assure that the layout is fully consistent with the initial schematics. Then a PG tape is generated and the ASIC can be fabricated by the ASIC foundry. The turn-around time to get prototypes is equal to the full process fabrication time since all the technological mask levels are specific to the circuit. Figure 2 shows the structure of a standard cell ASIC and Figure 3 the development procedure.

Figure 2

Figure 3

Note that because all the masks are to be produced in both the above methods, it is possible to combine them, designing the non critical parts of the design with standard cells and optimize the remainder with a full custom method.

3.2 The semi-custom approach
This technique consists of designing the circuit using prediffused matrices or products which are customized individually (PROM, FPLA) or at the very last steps of the diffusion process (gate arrays, linear arrays, component arrays).

This approach includes a large variety of prediffused parts differing amongst them by the size, the number of pads...

Only the necessary functions of the total die are customized, the others are left unused.

3.2.1 *Programmable devices FPLD*
Several functions are implemented on silicon, the connections between inputs and outputs are made through fuses (which can be burned) or diodes (which can be short circuited).

The function is achieved by programming the right fuses or diodes according to the type of programming.

3.2.2 *Arrays - The major part of this approach is devoted to gate arrays.*
As for standard cell approach, CAD tools are used intensively and designing a chip barely consists on assembling predefined functions.

Technically speaking, a function is defined by a particular interconnection of basic components grouped in cells, arranged in a matrix form.

The periphery of the matrix is used for input/output circuitry and power supply distribution.

Two families of gate arrays are to be mentionned.

1 - The cells are arranged in rows separated by free areas reserved for connections. These areas are called "routing channels" and are used by

the routing software to implement the connection wires between the cells. The gate array is said to have a "channelled architecture".

2 - The cells are arranged in contiguous rows such as a sea of gates. The gate array is said to have a "channelless architecture " or "sea of gates" architecture.

In this case, the routing software defines track of variables width above components (which will not be connected) adapted to the number of wires needed to achieve the cells connections.

There are generally five to ten different matrices for a gate array family, with a gate complexity matrix depending on the required number of gates, taking into account the "filling factor", that is the maximum number of usable gates over the total gate number of the matrix. This factor ranges from 50 to 80 %, depending on the logic functions to be routed, the efficiency of the routing software and the layout of the basic matrix.

Note : ROMs are included in this field since the programmation cannot be achieved by the customer but by the silicon founder.

The main advantage of a gate array is the short turn-around time for the design and the fabrication of prototypes.

For the design itself, the customer can use a library of cells developed by the gate array vendor. Those cells can be easily implemented using the basic devices of the array matrix. Thus, the customer can focus on the assembly and the interconnection of the gates necessary to its application, without being obliged to define the elementary gates as NOR, NAND, etc...

The ASIC designer gets a CAD system from the gate array vendor to develop his application : schematic capture, logic and timing simulator, router and checker. The router is a software specific to the gate array which automatically interconnects the cells of the array according to the "net list" resulting from the schematic capture.

The short turn-around time of a gate array comes from the fact that the matrices are fabricated in advance up to the first level of interconnection. Those wafers are called "base-wafers". Once the design of the interconnections corresponding to the application is done, only the interconnection levels have to be fabricated by the wafer foundry to get few prototypes for testing and validation. There are generally 4 technological levels used for interconnections, over a number of about 15 levels for the full process. The realization of those last 4 levels requires 3 or 4 weeks, a time shorter than the full process turn-around time of 8 to 10 weeks.

The figure 4 illustrates the basic structure of a gate array.

Figure 4

4 COMPARISON OF ASIC APPROACHES

It is interesting to compare the different ASIC techniques presented before, to show the main advantages of each approach and give the user choice criteria. The following table (figure 5) summarizes the comparison. It can be seen that the full custom approach should be used only when very optimized performance is required or when very high quantities are needed, implying a low production cost and then a small silicon area.

Figure 5

Programmable devices are usefull for breadboarding but are limited in terms of complexity and performance. In the other cases, a standard cell or gate array approach is better, either for design productivity or for prototype delivery time.

The ultimate choice between gate arrays and standard cells can be done considering the chip complexity and the quantities to be produced, as shown in figure 6. The standard cell technique is better for very high quantities due to its better intrinsic packing density silicon area savings lead to lower chip costs.

Figure 6

5. CONCLUSION

Whatever the approach chosen for the development of an application specific circuit, the ASIC based solutions which appeared in the past ten years has revolutionized the circuit design. Not only new, flexible high density silicon chips designs were made possible, but also highly productive and safe CAD tools allowed the user to get prototypes in a shorter time with a high probability of being right the first time.

The ASIC approaches could even benefit to the standard integrated circuit development as they

enable to drastically reduce the time-to-market while giving a fairly good packing density which continuously increases with the emergence of new powerful CAD tools.

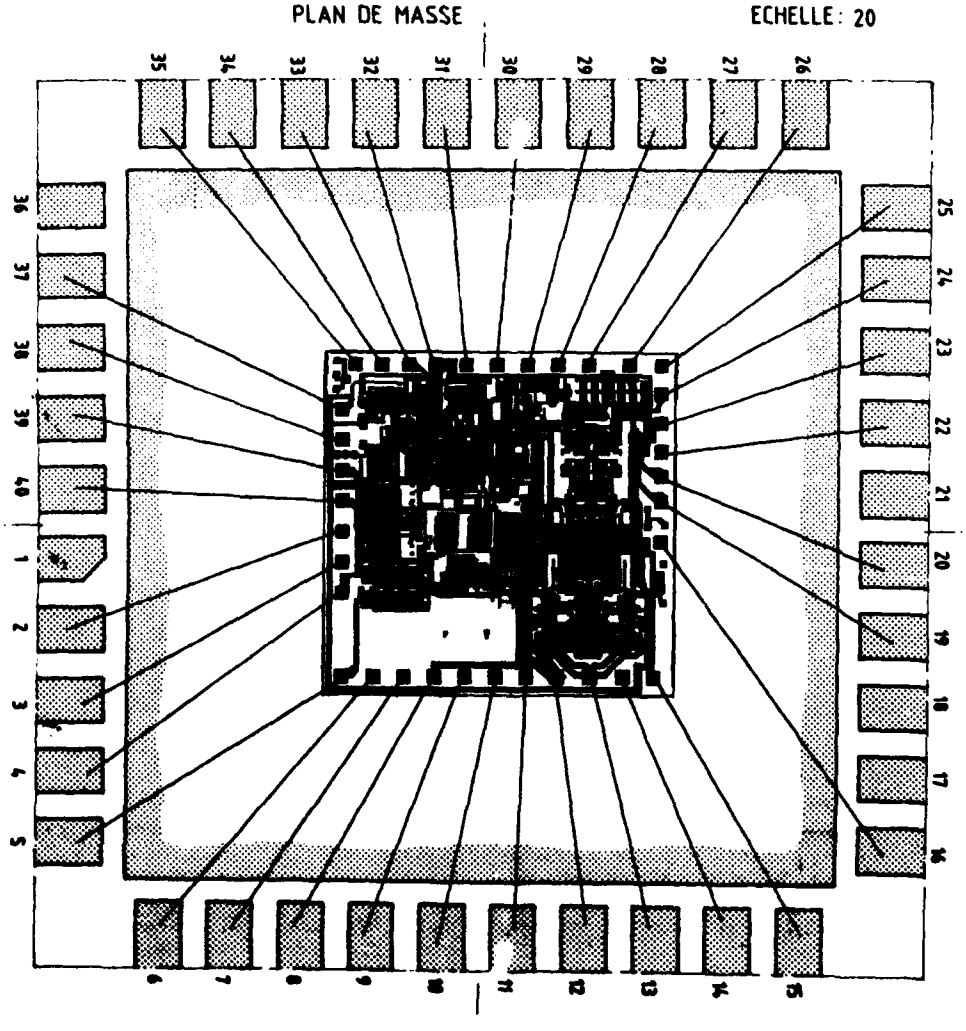

Figure 1

MIXED STANDARD CELLS AND RAMS

84 PINS

25K GATES

80 MM²

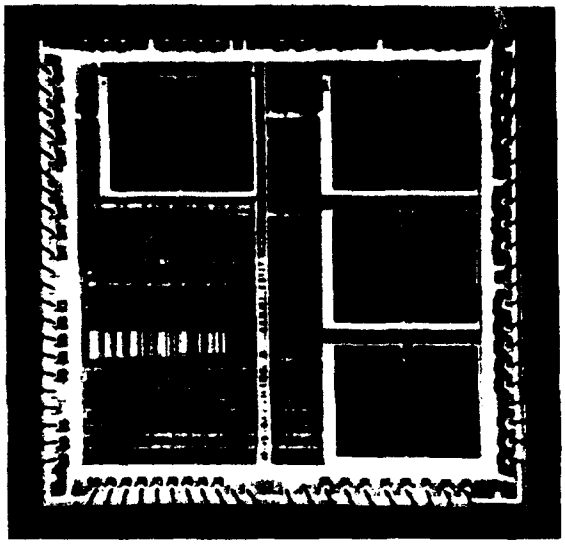

Figure 2

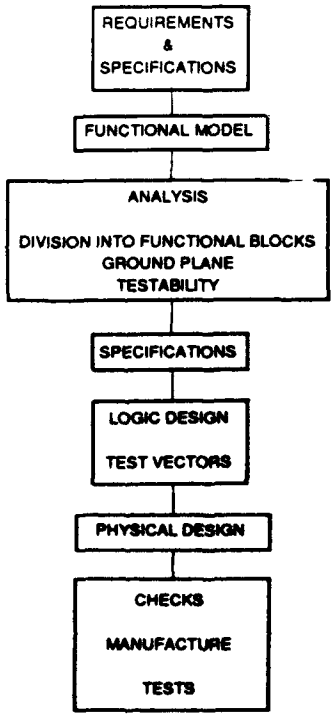

Figure 3

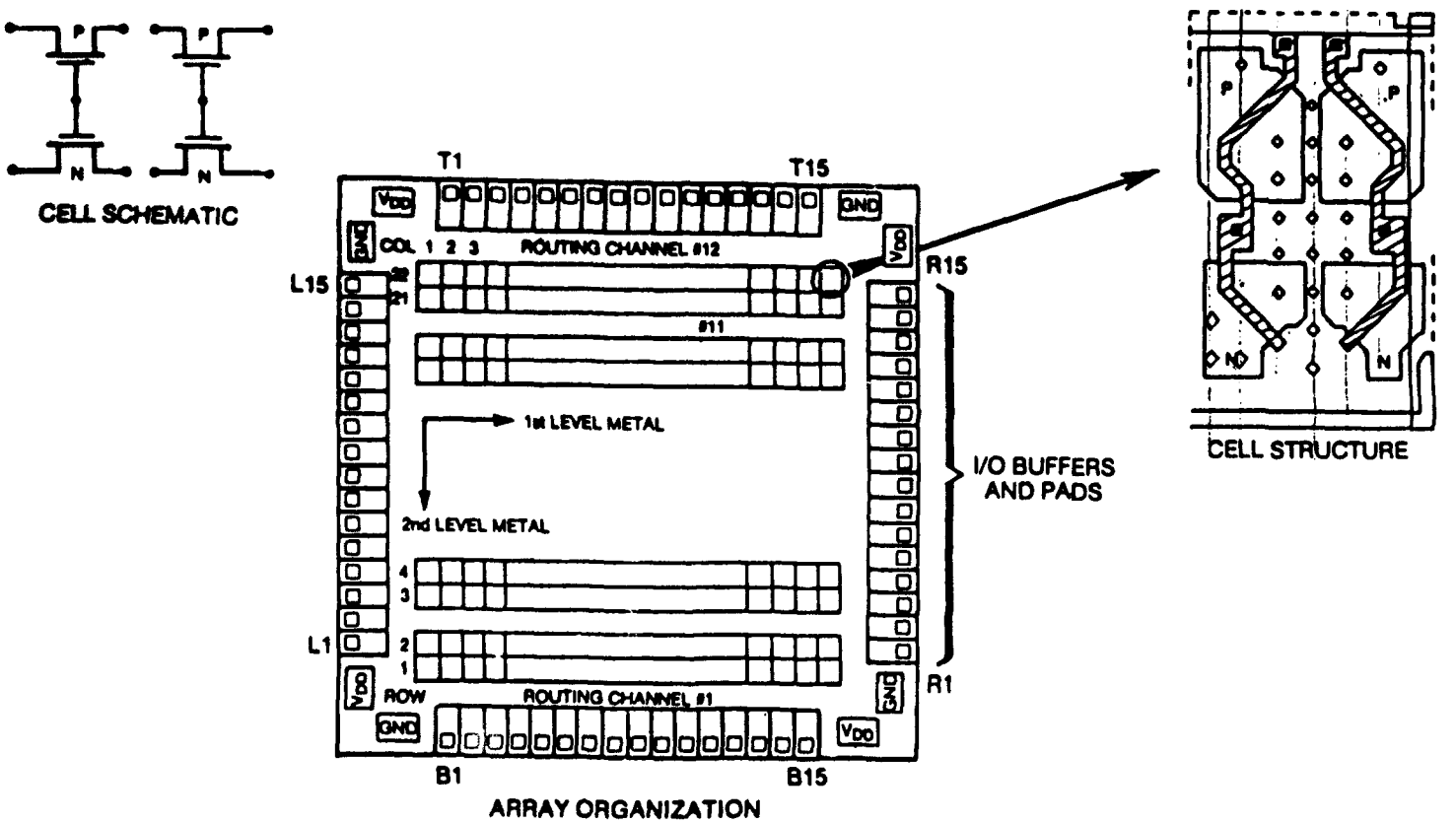
P
P
N
N
CELL SCHEMATIC
T1
T15
VDD
GND
COL 1 2 3
ROUTING CHANNEL #12
L15
R15
#11
1st LEVEL METAL
2nd LEVEL METAL
I/O BUFFERS
AND PADS
L1
R1
ROW
ROUTING CHANNEL #1
B1
B15
ARRAY ORGANIZATION
CELL STRUCTURE

Figure 4

	CUSTOM		SEMI-CUSTOM	
	FULL CUSTOM	STANDARD CELL	PROGRAMMABLE DEVICES	GATE ARRAY
Circuit function	Mainly linear Logic	Logic Mixed logic-analog	Logic	Logic Linear (component array)
Required performance (with respect to the technology capability)	Stringent Difficult circuits	Medium-high	Low	Medium
Complexity	Low (few 100 to 1000 components) Possibly high for logic	Very high 10k to 200k gates	Low	Medium-high 1k to 100k usable gates
Silicon area	Optimization requested generally small	Large (200 mm^2)	/	Large (50 to 200 m^2)
Packing density (component/mm^2)	Very good	Good	Poor	Medium
Prototype Turn-around time	8 to 10 weeks	8 to 10 weeks	2 days	2 to 4 weeks
Production cost (per gate or components)	Low	Medium	/	High
Design productivity	Low	High	/	High

Figure 5

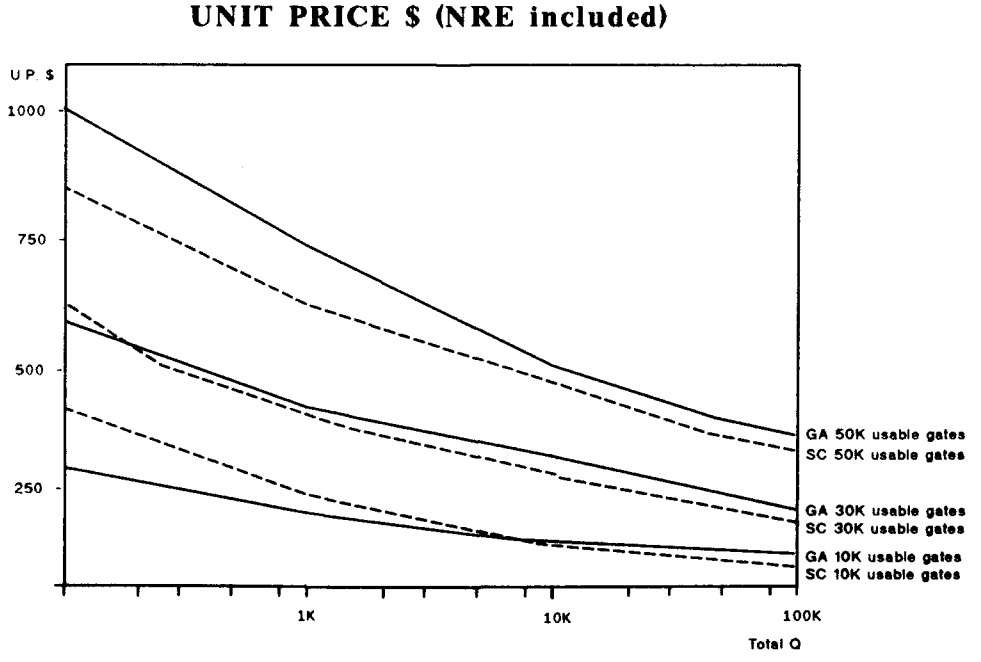

Figure 6

THE SILICON COMPILER FOR DESIGNING MILITARY VLSI ASIC's

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1. THE MILITARY ASICs OF THE NINETIES

It is well known that the cleverness and performance of a military equipment are packed in the silicon of the VLSI components which constitute a large part of it.

All Defense electronics manufacturers have understood this and design more and more complex and sophisticated specific circuits, in the digital area in particular.

By extrapolating the evolution of digital ASIC complexity since their emergence to the year 2000, the diagram of the figure 1 is obtained, showing that the one million gate level will be reached in 1995 and that ten million gate ASICs will probably emerge in the year 2000.

Figure 1

This evolution is mainly due to the advances of the silicon technology, whose both packing density and maximum allowable active area increase regularly, as shown in figures 2 and 3.

Figure 2

Figure 3

This integration capability is also highly dependant on the metal multilayer system which interconnects the transistors. The diagram of the figure 4 shows the ASIC complexity dependance on the number of interconnection layers.

Figure 4

The million gate complexity will necessitate at least four layers. The upper level will be first devoted to the power supply distribution. Then, when its pitch will be reduced to a value comparable to the lower layers, it will be possible to use it for routing any other signal, thus improving the packing density.

Another important characteristic of digital ASICs is their input-output number, which dramatically increases,as shown on figure 5. This evolution implies rapid advances in ancillary technologies such as assembly and testing.

In summary, the features of a military ASIC of the nineties will be :
- Gate complexity : 1 to 10 millions.
- Pad number : 500 to 1000.
- Operating frequency : 50 to 100 MHz.
- Testability : maximum fault coverage, JTAG norm.

Basically, it can be shown that the military needs, especially for avionic applications,often lead to the most complex ASICs achievable by the most advanced technologies, whereas civilian ASICs are less demanding, as shown on figure 6.

Figure 6

If the silicon technologies are capable of fast improvements, the question is to know wether the design techniques can follow this rythm or not.

Among the different design tools appearing on the marketplace, the silicon compilers are a promising solution.

THOMSON-CSF, with the support of the french ministry of Defense, chose this way in 1987 and launched a CMOS library development program using the GDT® compiler, and the GENESIL® environment. The major interest and features of this approach are detailed in the following chapters.

2. WHAT IS A SILICON COMPILER ?

2.1 Operation principle

A silicon compiler is basically an algorithm : it is a software, written in a high level langage (C for instance), which delivers, when executed, the different representations of the

logic functions specified by the user, for his application.

Unlike the standard cell libraries, there is no longer a data base of fixed logic blocks, but a group of algorithms, called generators, which give the user the logic functions necessary for the design of an ASIC, from the most simple to the most complex ones : I/O interface, flip-flop, memories, PLA, data path, etc...

The figure 7 presents the basic structure of a function compiler in its environment.

Figure 7

The compiler itself is composed of five algorithms or generators which give the five logic function representations needed for specifying, simulating, checking and fabricating an ASIC :

- The icon generator gives a symbol of the fonction. This symbol will be used for the ASIC schematic capture phase.

- The behavioral model generator gives the logic simulation model of the function for simulating the entire ASIC before and after the place and route phase of the design.

- The electrical model generator delivers a transistor level description of the logic function for timing simulations.

- The boundary box generator gives the physical boundaries of the compiled function, with the location of inputs, outputs, power supply rails.

These boxes will be used by the place and route software to constitute the final ASIC.

- The layout generator delivers the graphical data of all devices and connections of the function embedded in the boundary box.

It has been established that a function generator is in fact a set of algorithms which are executed on request. Those softwares need two types of information to be operated :

- Technological data related to the fabrication process chosen by the user : design rules, simulation parameters, etc... These informations are stored in the technology files. There is one file per process.

- User informations, specifying the features of the desired function : number of bits of a SRAM for example.

These characteristics are chosen by the user thank to a menu associated to each generator. This menu, once called and executed, delivers the particular representations of the specified function, called an instance.

2.2 Interest of the silicon compiler

The major advantages of the silicon compiler approach are as follows :

Technology independance :
The generators are softwares which define a logic function, even a very complex one, by algorithms fully independant from the target technology. So, a given generator can deliver many instances relating to many different technologies, to the user request, among those which have been described in the technology files.

Horizontal and vertical portability :
These concepts directly stem from the technology independance. They are described in figure 8.

Figure 8

If several technologies of the same generation (same critical dimensions) are described in the technology files, a logic function can be compiled with each of them, leading to identical instances from a logical stand point, but each of them fitting to each technology. The function is "horizontally ported" as the layout rules and performance are at the same level.

If two processes, one of the n generation (1.2 µm CMOS for example) and the other of the n+1 generation (0.8 µm CMOS) are described in the technology files, the compilation will lead again to two instances of the same logic function, but with the performances of each process in term of density and speed. This function is vertically ported from the n generation process to the more performant n+1 one.

Design productivity :
An instance generation requires the execution of an algorithm on a computer, in a relatively short time, negligible with respect to the time needed for definition and specification of the logic function. The generation of layout and model data base is greatly reduced, which

contributes to increase the design productivity.

Design safety :
Once fully validated, each function compiler can give many instances without any error, in the limits of its parameterization capabilities. In the classical design flow of IC's the circuit definition is carried out with a top-down process and is followed by a bottom-up building process. The major design effort of this latter phase lies in the consistency checking between the specified circuit and the built circuit.

Thanks to the silicon compiler, which delivers high level, optimized functions, with fully consistent descriptions, the designer can focus on the optimized association of those functions, very early in the design flow and with the best abstraction level. The design methodology imposes stringent checking phases at the end of the design to eliminate the last errors.

2.3 Structure of a function compiler
From a structural stand point, a function compiler is a hierarchical assembly of elementary objects. These ones (transistors, connections, contacts...) are grouped to constitute elementary cells, called leafcells, which are a basic logic function (Nand gate, memory cell). These leafcells are in turn assembled to give more complex functions. The power of the silicon compilation lies in the langage enabling this hierarchical assembly.

This universal langage allows the library designer to describe both the graphical and electrical objects. The description consistency is assured through this unicity.

The figure 9 shows an example of an inverter leafcell with the associated code.

Figure 9

The dimensions and the location of the leaf cell objects can be specified either in absolute values or as a function of the design rules described in another file. Should this file be changed, the function would be compiled in a new technology.

This mecanism leads to the technology independance of the leafcells and enables a fully automated porting process to several technologies.

As the full parameterization of the leafcells is very complex, it is often better to describe them in absolute values. Then partially automated processes to adapt the leafcells to existing technologies have to be developped.

As far as the generators are concerned, it is always interesting to assemble the leafcells in a procedural way.

The figure 10 shows a n bit register generator using this technique and a particular instance with n = 2.

Figure 10

The leafcells are represented by their boundaries and their access points. This example also shows how user parameters (the number of bits of the register) can be used in the generator to make it able to compile many different functions.

2.4 Calibration of a compiled function library
When the ASIC vendor wants to offer its compiled function library in a given technology, he has to calibrate or to port the library on this technology. The main tasks of the calibration process are the following :

- Description of design rule files. Those design rules are used as parameters in the procedural descriptions.

- Validation of the generator operation with the new technology files.

- Description of the object electrical parameters which will be used for simulating the electrical behavior of the circuits created by the generators.

- Electrical simulation of a set of representative function instances to determine the timing parameters used in the behavioral model generators. Those timing parameters are described in separate files, which makes the generators technology independant.

- Experimental validation on silicon of test circuit including main function instances and reliability test bars.

2.5 Compiled function library content
For fully benefitting from the advantages of a silicon compiler, the library shall include, not only a standard cell set, but also high level macrofunctions providing a high packing density and top performances.

The library developped by THOMSON TMS includes :

- Standard cell compiler.
- Static RAM compiler (single port, multi-port).
- ROM compiler.
- PLA compiler.
- Multiplier compiler.
- Bit-slice microprocessor compiler from 1 to 32 bits.
- Sequencer compiler.
- Data path compiler : this macrofunction allows the user to synthetize complex data flow processing circuits, with a sublibrary of 30 generators (registers, ALU's, FIFO's...).
- Interface circuit compiler enabling all CMOS and TTL input or output combinations, with a JTAG boundary scan option according to the IEEE 1149.2 norm.

A tap controller compiler comes with the boundary scan option.

2.6 User environment

A silicon compiler must be used with an efficient, complete software environment to be fully profitable to the designer.

The user environment of the TMS library is shown in figure 11. There are :

Figure 11

- A definition environment for specifying the logical options and the parameters of the compiled functions to be instanciated.

- A validation environment with :
  . A logic simulator for behavioral and timing simulations.
  . A timing analyser for identifying and measuring the critical paths.
  . An automatic test pattern generation tool for generating the test vectors with a good fault coverage.
  . A fault simulator for fault coverage measurement.

- A building environment including, in addition of the macrofunction generators :
  . A data path compiler.
  . A place-route software for standard cells.
  . A peripheral interface compiler for I/O's implementation.
  . A global place and route tool for assembling all the blocks constituting an ASIC.

3. ASIC DEVELOPMENT WITH A SILICON COMPILER

The previous chapters showed the operating principles of a silicon compiler along with the associated user environment. This chapter will deal with the design methodology and the associated design flow utilized to get silicon prototypes.

The typical design flowchart is given in figure 12.

Figure 12

The main stages are the following :

1. To formalize the ASIC specifications and an associated test sequence.

2. Circuit definitio ading to a schematics and to a floor ining of the logical function instances.

3. Schematic simulation and timing analysis.

4. Test sequence generation. The test sequence developped in stage 1 is complemented to get a sufficient fault coverage (at least 95 %). A number of "design for testability" rules have to be respected to get this minimum fault coverage. The industrial testing constraints are also taken into account at this stage of the design.

5. ASIC building by placement and routing of the schematic instances.

6. Design checking by simulation and timing analysis taking parasitic elements into account.

7. Final checking. This operation, realized by the ASIC vendor, includes :
   - Design verification :
     . conformance to layout rules,
     . consistency between behavioral and transistor level simulation.
   - PG tape generation.
   - Test program generation from test sequences given by the designer.

The completness of those verifications leads to a "right the first time" rate very close to 100%.

4. EXAMPLES

THOMSON TMS developped many ASICs with their compiled function library. The complexity of these circuits ranged from 10K to 85K gates, using a 1.2 μm CMOS technology.

Two circuit categories must be considered :

- The *pad limited* circuits : the chip area is determined by the number of I/O's (more than 300 in 1990).

- The *core limited* circuits : the chip area is given by the packing density of the process.

The maximum complexity of an ASIC is also determined by its architecture and by the logical functions used : an ASIC using mainly memory blocks will be 3 to 4 times denser than another ASIC using only random logic. Few examples of digital ASICs for military applications are given hereafter :

- Circuit "A" (figure 13) is a DSP ASIC.

- Circuit "B" (figure 14) is a high rate communication control circuit used for processor exchange protocols. It has more than 300 pads.

- Circuit "C" (figure 15) is a radar signal processing circuit.

- Circuit "D" (figure 16) is a specific memory management unit. It is the most complex circuit realized with the 1.2 µm CMOS technology.

The following table summarizes the main features of these ASICs :

	"A"	"B"	"C"	"D"
Die size (cm^2)	1,7	1,84	0,8	1,02
Complexity (transistors)	260.000	260.000	200.000	315.700
Frequency (MHz)	21	16	16	12,5
Computation power	500 MOPS	320 Mb/s	50 MOPS	160 Mb/s
Power consumption (W)	4	2	0,5	2

All the ASICs realized with GDT/Genesil® have been fully functional at the 1st silicon stage. This confirms the design security of the silicon compiler approach.

The design productivity ranged between 150 and 200 gates/designer/day, which enables to maintain the development time below 9 to 12 months for most complex ASICs.

5. THE FUTURE OF THE SILICON COMPILER

The silicon compiler approach implies three development areas :

1. CAD tools for definition, simulation and compilation of ASICs.
2. Library of compiled functions.
3. Technologies.

Today, it is clear that the most significant advances will come with the CAD tools and silicon processes. The libraries themselves have benefited from large amount of R & D and are now of a high level of performance. But the limitations encountered in the ASIC development are due to two main problems :

- The high complexity of the new circuit architectures and the absolute necessity to exhaustively simulate the entire circuit impose the development of new CAD tools to assure a continuous increase of the design productivity.

- The fabrication of these ULSI ASICs will be very demanding to the technologies : critical dimension reduction, increase of the number of interconnection layers and of the maximum chip size, etc...

Nevertheless, the second point is not a bottleneck as the "evolution capability" of silicon processes is well known. The emergence of new technologies can be accurately predicted, at least for the next decade. So, by continuously porting the libraries on the best emerging processes, it will be possible to assure the best service to the ASIC users, in term of silicon.

The quality of the service to the ASIC user's will greatly depend on the new CAD tools of the user environment :

- **Logic synthesis is already available. It allows the designer to automatically create a logic schematics from the behavioral model, bringing a large improvement of the design productivity in the definition phase.**

- **Architecture synthesis which automatically creates the block partitionning of the circuit from its global behavioral model.**

- Test assistance tools will be considerably improved as the time devoted to the more and more complex test pattern generation must remain as short as possible. The new tools will be able to operate hierarchically for the testability analysis and the test pattern generation.

- The place and route tools will handle 3, 4 and even more interconnection layers.

- The most important evolution will be the emergence of the framework concept. This concept will give the user an open environment, able to accept many different specialized softwares, whilst maintaining the global integration necessary for a good design efficiency.

All those ways of improvement show the large potential of advances achievable in the CAD tool field, to better satisfy the needs of the ASIC designers of the nineties.

The design productivity will continue to grow according to the curve of the figure 17, and will reach the level of 1000 gates per designer per day probably in 1993. The 10000 gates per designer per day could be reached before the year 2000.

Figure 17

In the future, there is no doubt about the ability of silicon compilers to handle many other technologies, as bipolar or GaAs, with as much efficiency as for CMOS technology. Then, the silicon compilation will have reached its full maturity.

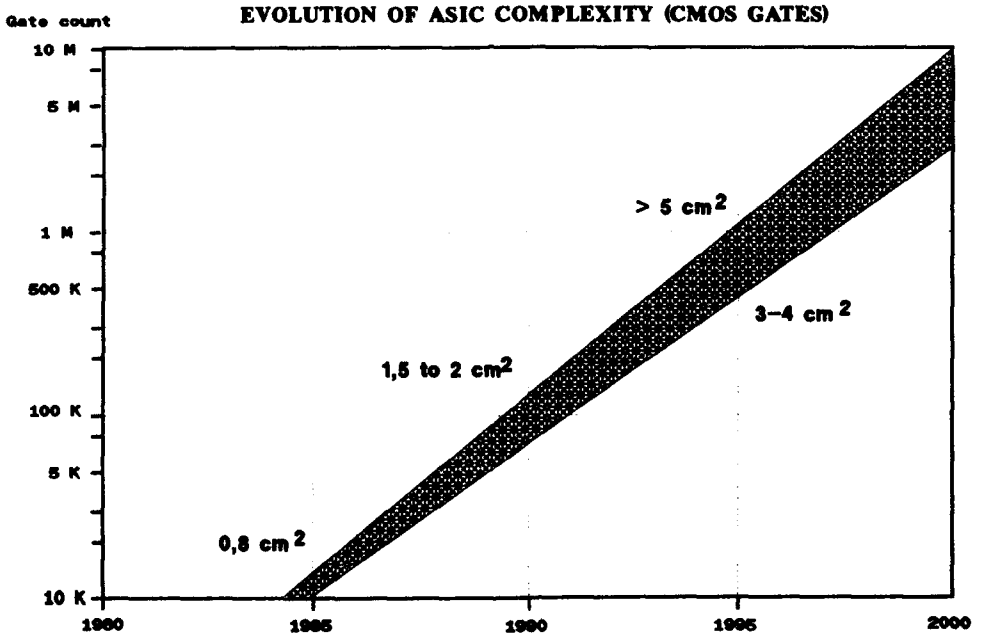


Figure 1

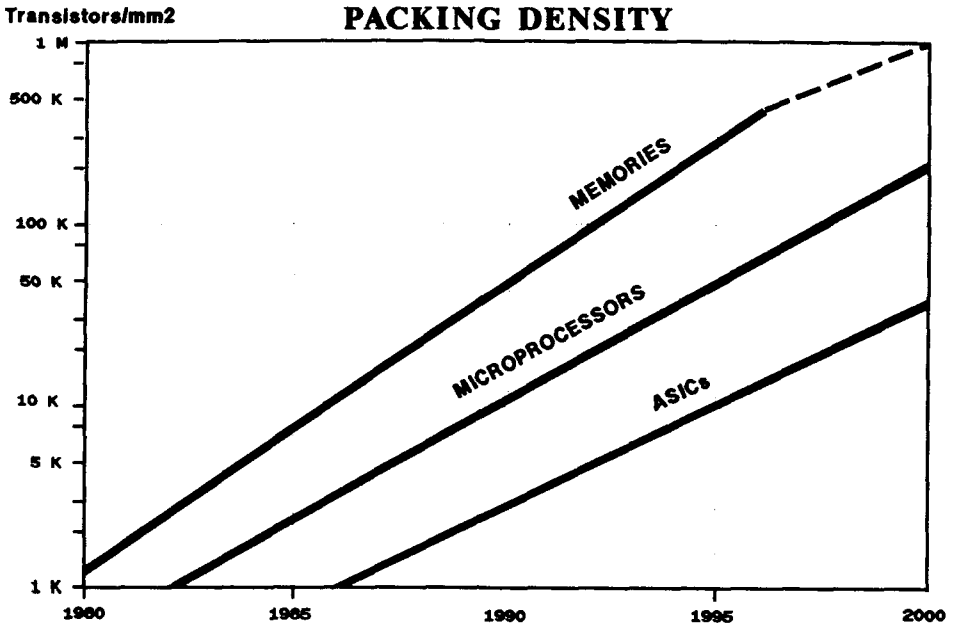


Figure 2

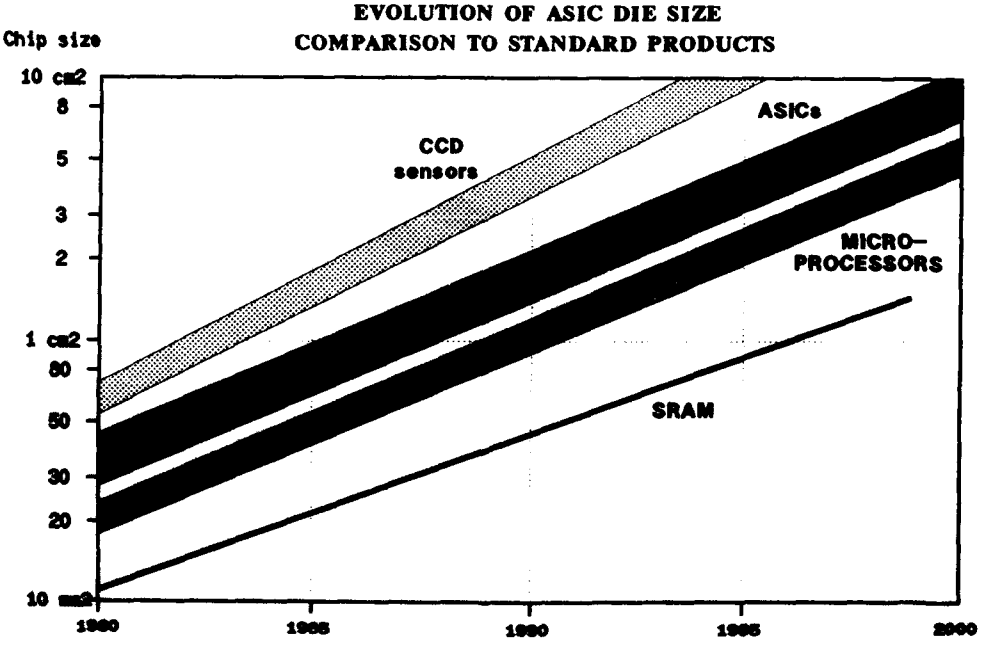


Figure 3

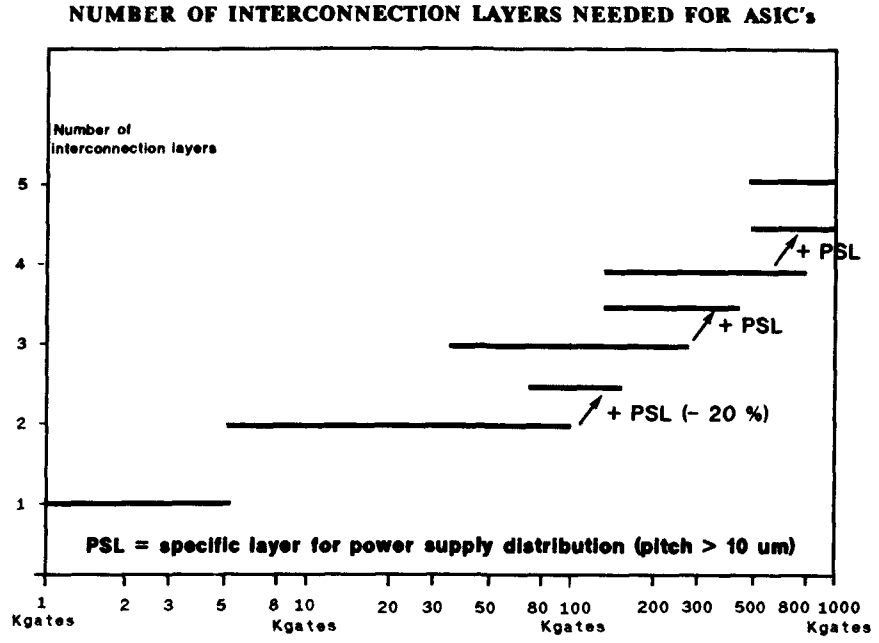


Figure 4

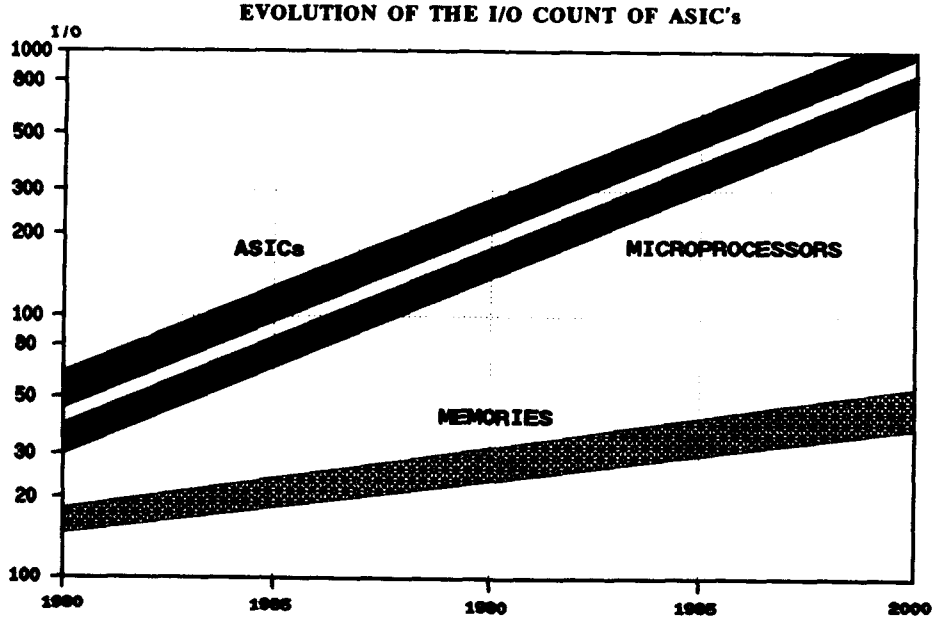


Figure 5

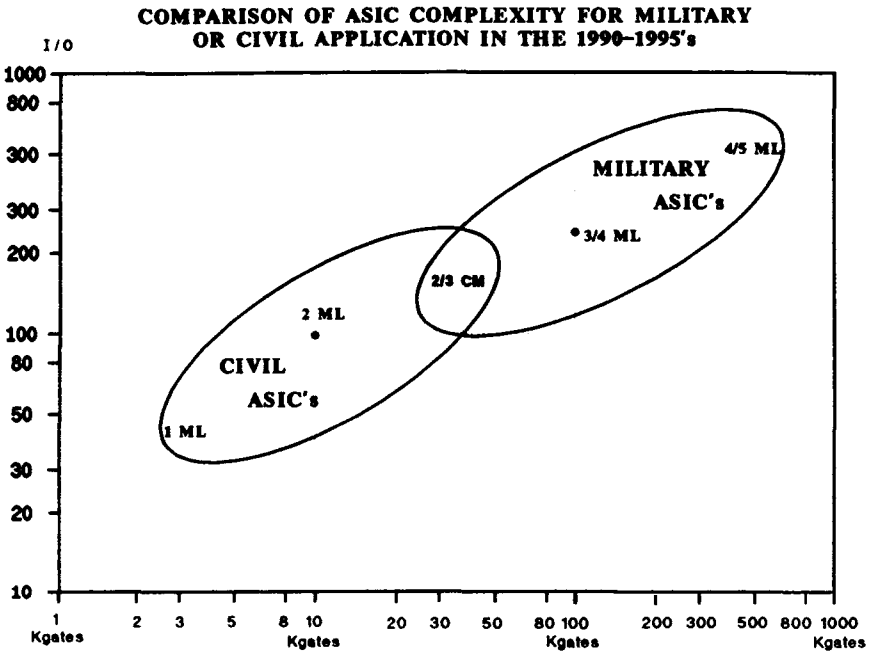


Figure 6

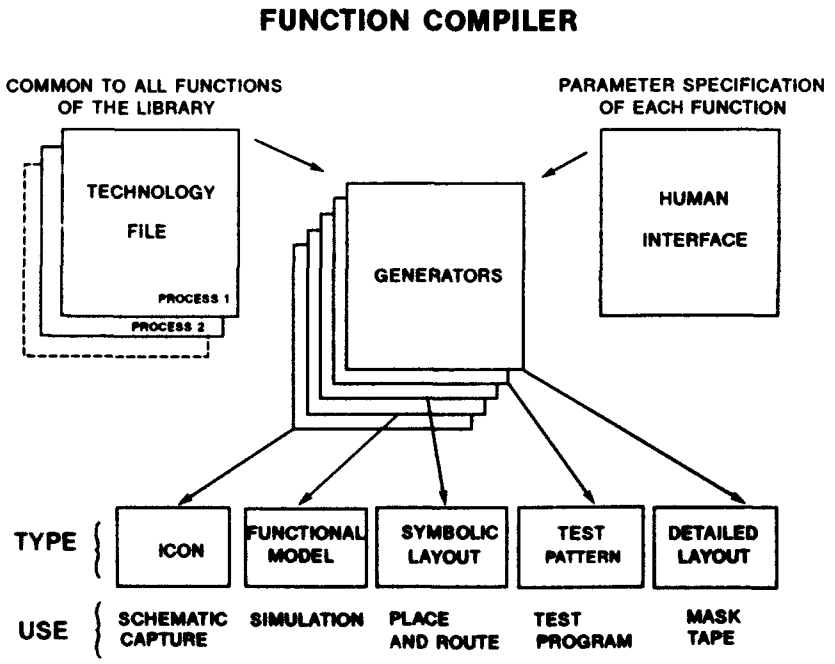
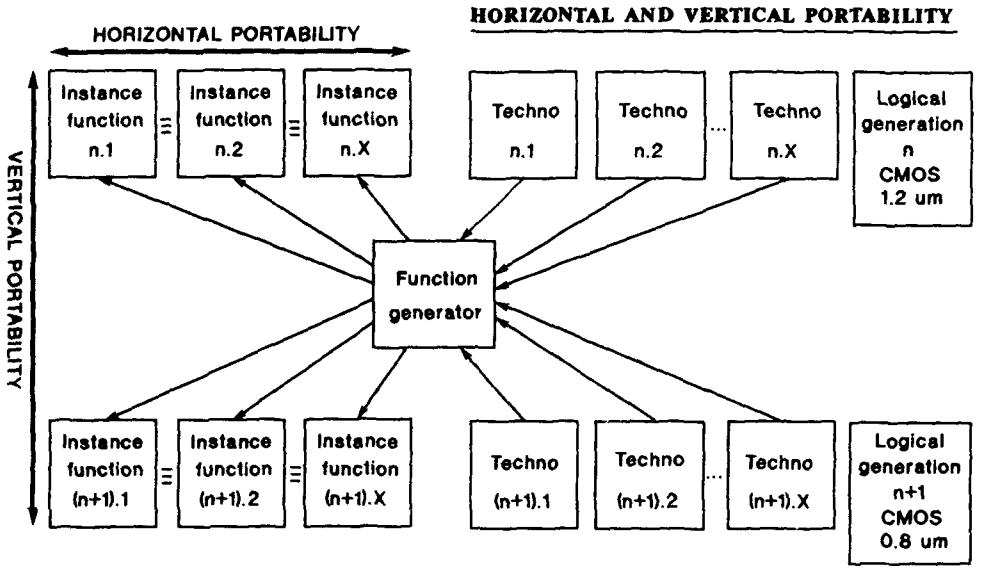


Figure 7



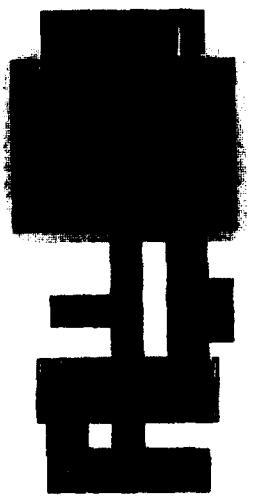
The instances n.1, n.2, n.X have the same logical function with comparable performances, given by the technology generation # n.

The instances (n+1).1, (n+1).2, (n+1).X also have the same logical function, but the performances are better, benefitting from advances of the technology # n+1

Figure 8

INVERTER LEAFCELL GENERATOR

Generated instance for
lg = 3, pw = 12, nw = 6



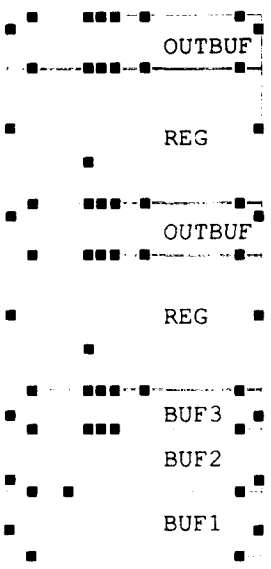
Code showing the parameterization of transistor sizes (gl, pw, nw)

```
L: TECH ANY
CELL inv_G ( pw=12, nw=6, gl=3 )
{                                          pw : P channel width
# bbox: ll= (-6,-2) ur= (63,82)            nw : N channel width
# 6 terminals                              gl : gate length
  IN POLY input W=3 (0,40) ;
  VDC MET1 vdd_l W=4 (0,80) ;
  VDD MET1 vdd_r W=4 (40,80) ;
  GND MET1 gnd_l W=4 (0,0) ;
  GND MET1 gnd_r W=4 (40,0) ;
  OUT POLY output W=3 (60,40) ;
  NODE POLY p3 W=3 (20,40) ;

  TP t0 R90 W=pw L=gl (20,60) ;
  TN t1 R90 W=nw L=gl (20,20) ;

  MPDIFF c0 R90 W=pw (40,60) ;
  MPDIFF c1 R90 W=pw (0,60) ;
  MNDIFF c2 R90 W=nw (40,20) ;
  MNDIFF c3 R90 W=nw (0,20) ;
  MPOLY c9 (60,40) ;

  PDIFF t0.d VER LEFT=15.5 c1 ;
  NDIFF t1.s VER RIGHT=15.5 c2 ;
  NDIFF t1.d VER LEFT=15.5 c3 ;
  MET1 vdd_l VER RIGHT=40 vdd_r ;
  MET1 c1 HOR UP=20 vdd_l ;
  MET1 gnd_r LEFT=40 VER gnd_l ;
  MET1 gnd_l UP=20 HOR c3 ;
  PDIFF c0 LEFT=15.5 VER t0.s ;
  MET1 c9 LEFT=20 DOWN=20 c2 ;
  MET1 c9 TRUNC LEFT=20 UP=20 c0 ;
  POLY output HOR VER c9 ;
  POLY W=gl p3 DOWN=20 HOR UP=6 t1.gl ;
  POLY W=gl p3 VER HOR UP=11 t0.gl ;
  POLY input RIGHT=20 VER p3 ;
COMPACTXY;
}
```

Figure 9

N BIT EXPANDABLE REGISTER GENERATOR

Generated instance for nbit = 2



Code showing the parameterization of the bit number

```
                                                    ## REGISTRE EXTENSIBLE N BITS
                                                    ##
CELL REG_G (nbit    ) ;

IF (!EXISTS (BUF1)) CALL BUF1 CELL buf1 () ;        ##
IF (!EXISTS (BUF2)) CALL BUF2 CELL buf2 () ;        ##  APPEL DES SOUS CELLULES
IF (!EXISTS (BUF3)) CALL BUF3 CELL buf3 () ;        ##
IF (!EXISTS (REG)) CALL REG CELL reg () ;           ##
IF (!EXISTS (OUTBUF)) CALL OUTBUF CELL outbuf () ;

INST buf1 buf1 (0,0) ;                              ##
INST buf2 buf2 ;                                    ##  INSTANTIATION DES BUFFERS ENTREE
INST buf3 buf3 ;                                    ##

buf2.vdd_l AT buf1.vdd_r ;                          ##          PLACEMENT DES BUFFERS
buf3.vdd_l AT buf2.vdd_r ;                          ##          PAR ABUTTEMENT DE TERMINAUX

NUM i=-1 ;                                          ##  INSTANTIATION DES REGISTRES
WHILE (++i<nbit) {                                  ##  PLACEMENT PAR LES TERMINAUX DE VDD
                                                    ##  POUR NBIT (ABUTTEMENT)
    INST reg reg[i] ;
    INST outbuf outbuf[i] ;

    IF (i != 0) {                                   ##  PLACEMENT AVEC CAS PARTICULIER
        reg[i].vdd_l AT buf3.vdd_r ;                ##  DU PREMIER REGISTRE
        outbuf[i].vdd_l AT reg[i].vdd_r ;
    }
    ELSE {
        reg[i].vdd_l AT outbuf[i-1].vdd_r ;
        outbuf[i].vdd_l AT reg[i].vdd_r ;
    }
IN MET2 rn_d AT buf1.rn_d ;                         ## AJOUT DES TERMINAUX POUR LA PROPAGATION
IN MET2 rr_u AT buf1.rn_u ;                         ## DES INFORMATIONS ELECTRIQUES

IN MET2 rn_d AT buf2.rn_d ;                         ## DEPUIS DES TERMINAUX D'INSTANCES
IN MET2 ck_u AT buf2.ck_u ;                         ## AUX TERMINAUX DE LA CELLULE TOP

IN MET2  d_d AT buf3.d_d ;
IN MET2  d_u AT buf3.d_u ;

} -i ;
WHILE (++i < nbit) {
    IN MET2 rn[i]_d AT reg[i].rn_u ;                ## PLACEMENT DES TERMINAUX
    IN MET2 rn[i]_u AT reg[i].rn_d ;                ## DES REGISTRES

    OUT MET2 q_u[i] AT outbuf[i].tbout_u ;
    OUT MET2 q_d[i] AT outbuf[i].tbout_d ;
```

Figure 10

DESIGN ENVIRONMENT

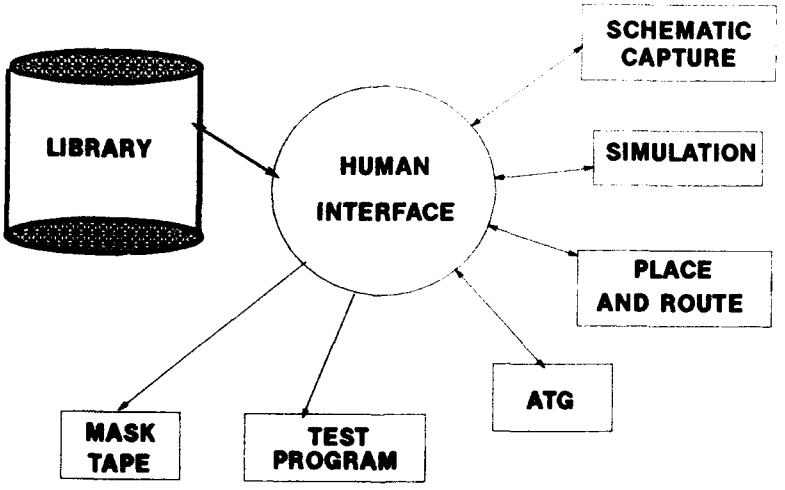


Figure 11

DESIGN FLOW

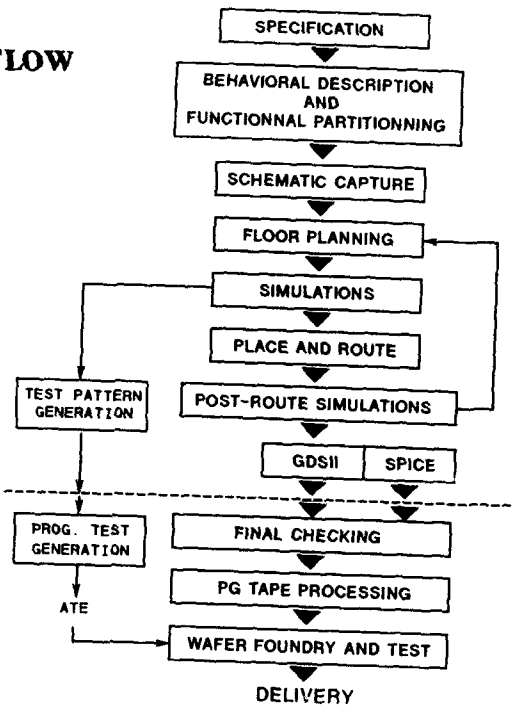


Figure 12

"Circuit A"

170 mm2

260 K TMOS

91 signals

PGA 107

179 pads

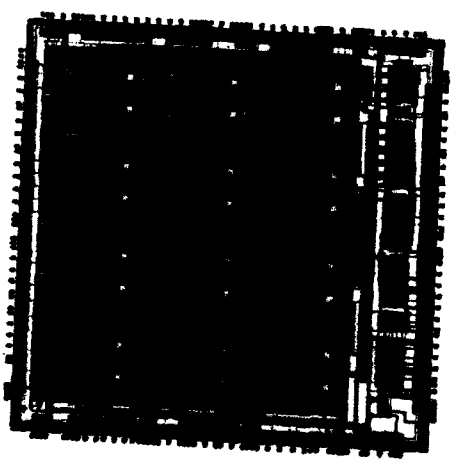


Figure 13

"Circuit B"

243 I/O's

184,000 transistors

180 mm^2

HCMOS3 technology

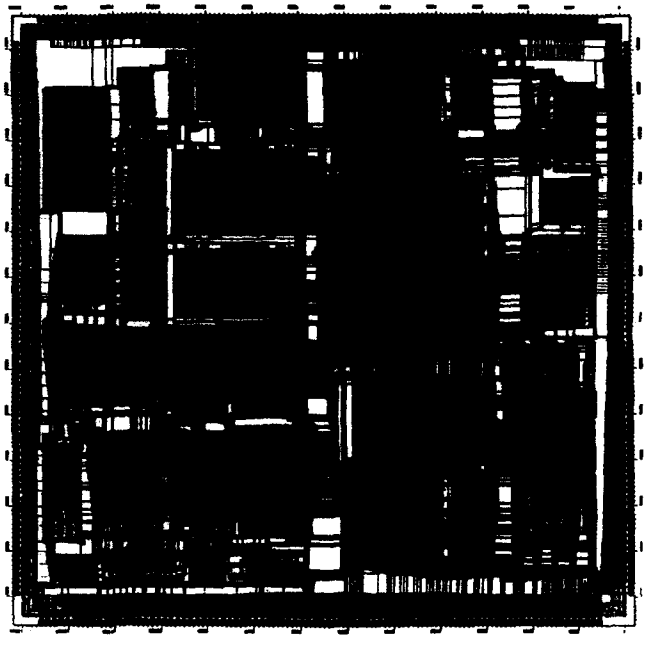


Figure 14

"Circuit C"

0.8 cm^2

200,000 transistors

16 MHz

0.5 W

Video treatment

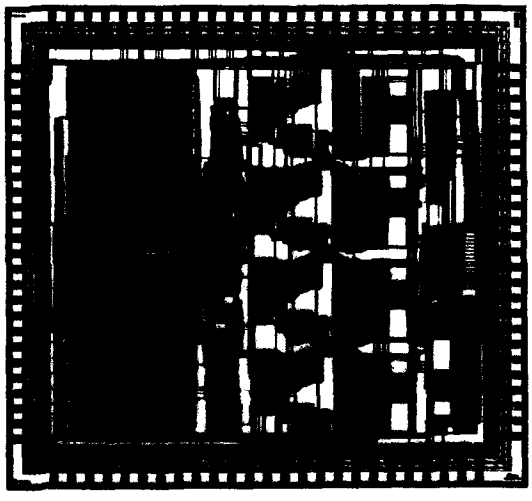


Figure 15

"Circuit D"

1.02 cm2

315,700 transistors

12.5 MHz

2 Watts

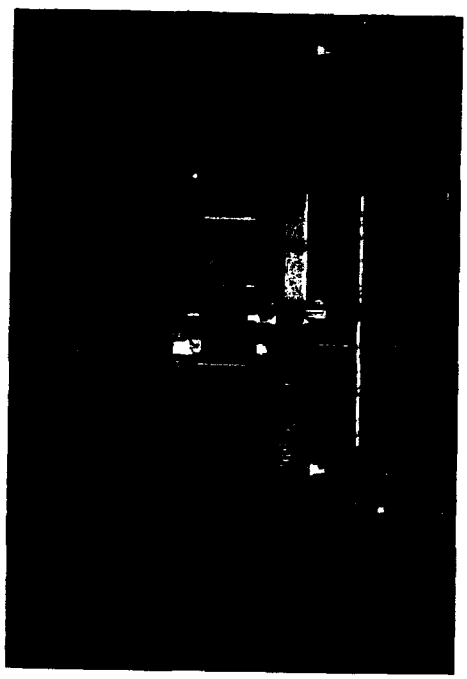


Figure 16

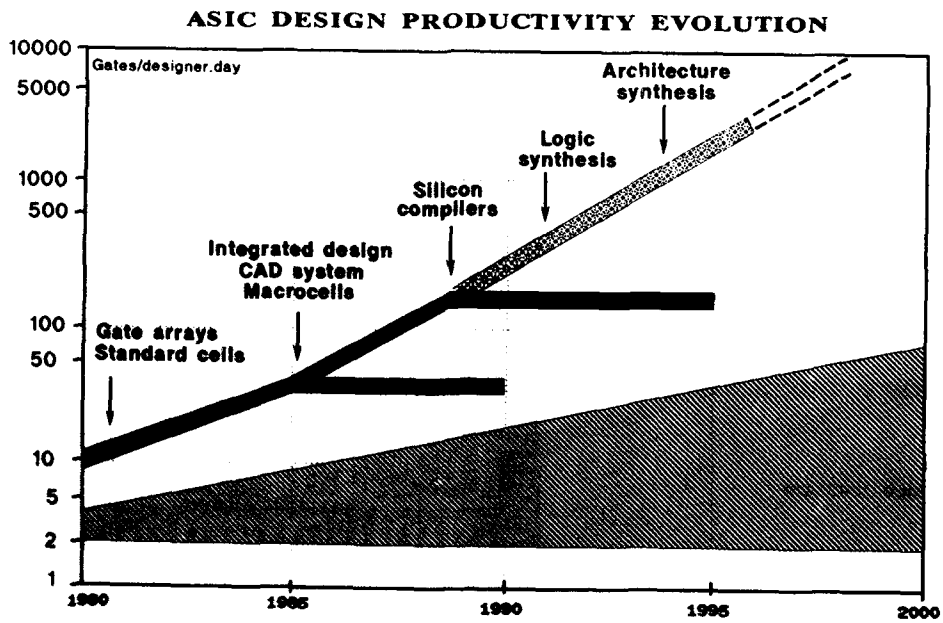


Figure 17

APPLICATIONS OF SILICON HYBRID MULTI-CHIP MODULES TO AVIONICS

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1. SUMMARY

Silicon-based MCMs are an inevitable concomitant of reduced feature size and higher speed IC devices.

Early versions are available and are being exploited in military and high performance commercial applications. Their use will proliferate rapidly over the next four years and is likely to extend the use of monolithic ICs into performance areas which were previously inaccessible.

MCMs are application specific and their functional density is comparable to that obtained with wafer scale integration. Yet MCMs permit the integration of several different technologies and passive components. They can even be made self-testing. In this sense they have opened the way to the ASIM - the application specific integrated module.

Wafer scale integration provides a single-process system-on-a-chip. The clock frequencies will be higher than in an MCM because all interconnects are on-chip. However, their restriction to a single basic process means that MCMs have much greater flexibility of application. There are uses for both types of device.

2. GENERAL BACKGROUND

A multi-chip module, MCM for short, is an assembly of semi-conductor chips (usually naked) and discrete components on a substrate with high density interconnect.

The assembly is packaged as a single part.

MCMs are usually classified as L-type, C-type or D-type according to the technology used.

L-type MCMs use laminated pcb's.
C-type MCMs use ceramic substrates.
D-type MCMs use deposited metal interonnect with polymeric or thin film dielectrics.

Silicon hybrid MCMs are D-type devices using silicon as the substrate material. This chapter is devoted to D-type MCMs. Use of MCM without qualification implies the D-type form.

Work on D-type MCMs started about 10 years ago but has intensified over the last 5 years. In 1988 at least 12 companies in the US, 6 in Japan and 11 in Europe were engaged in MCM R & D, and currently there are at least 50 participants world-wide.

The push towards MCMs derives directly from devolopments in VLSI technology. Their introduction is as crucial to the development of VLSI performance as was the jet engine to the development of aircraft performance.

In VLSI the ultimate technology drivers are the steady reduction in minimum feature size and the equally steady growth in the chip size which can be exploited commercially in VLSI devices.

Figure 1

Reduced feature size results in more closely packed active devices and shorter average interconnect lengths. Limiting signal skew then occurs at higher clock frequencies. Reducing feature size therefore results in a steady increase in the maximum operating frequencies of the chips themselves.

Figure 2

However the package containing the chips cannot be packed much more closely than they are packed already.

This limitation of existing assembly techniques will stunt the potential growth in system speed unless radically new assembly methods are introduced.

Reduced feature size and increased chip size combine to give increasing chip complexity. The growth in the number of equivalent gates

per chip, fig. 3, shows this effect with time. There is a well known realtionship (Rents Rule). Fig. 4, between gate count and the number of contact pads required round a chip. So far, these pads have been arranged around the periphery of the chip. As logic density goes up, the pad requirement, following Rents Rule, increases exponentially. With imminent developments in device technology the pad count can easily be more than double the pad capacity of the chip periphery.

Figure 3

Figure 4

Even if the chip limitation is circumvented the same problem will re-emerge at the package. Microprocessor based systems with wide parallel highways aggravate the problem.

Functional density in an MCM is comparable to that in wafer-scale integration yet permits different technologies freely to be mixed. Single chip packaging within systems will becoma impractical in near term advanced system design and multi-chip assemblies will become mandatory for high performance systems of all types. In time, like all new technologies, costs will be reduced to a level where MCMs are widely adopted because of their many advantages rather than through the force of necessity.

All the advantages benefit aerospace applications. Avionics is likely to be among the first technologies to adopt MCMs rather than having them imposed upon them.

3. THE ADVANTAGES OF SILICON HYBRID MCMs

Silicon is a particularly good substrate material for many reasons. Its use is the basis for most of the advantages of this form of MCM. It is widely available and inexpensive. It has good thermal conductivity and a temperature coefficient of expansion (TCE) identical to the chips attached to it. The processing of the material and the inteconnect technologies are well understood and capable of high yields. The surface finish of the substrates is very high and will accept closely pitched fine lines of interconnecting metal.

It has one other potential advantage, not possessed by any other candidate substrate material. Active devices can be diffused directly into the substrate. Silicon MCMs have inherent 3D assembly capability.

The specific advantages of MCMs are :

- They have higher clock frequencies because system operating speed is matched to the high chip operating speeds.

Figure 5

- They are more reliable because the average power per clock cycle is reduced, there are fewer packages and many fewer package pins.

- They are smaller because the chip packaging density is higher.

Figure 6

- They are cheaper than discrete component and pcb construction at higher chip densities. The break-even point will fall rapidly as MCM output accumulates.

Figure 7

All these advantages accrue when using standard chips. Further gains can be achieved by using ASIC methods. The power levels in the output drivers on the chip can be reduced. This will also lead to a reduction in chip size. Any high power drivers for long interconnect of for out-of-package interconnect can be put in the substrate so that the smaller chip size is retained. The result is smaller area, reduced power demand and lower operating temperatures.

There are two ways of connecting the chip to the substrate. One is conventional TAB or wire bonding with the chip attached to the substrate face up.

The second way is to use a flip-chip method with the chip assembled face down. This type of assembly allows contact pads to be disposed anywhere on the chip's surface. Long runs of interconnect can then be avoided between a particular circuit node and a peripheral bond pad. The result, again, is smaller size and reduced power drain.

Flip chip assembly has another advantage. Flip chip bonds have much lower inductance than bond wires. Substrate operating frequencies can be raised by using interconnect with transmission line characteristics. Inductance

then becomes as important as capacitance is at lower frequencies.

However, flip-chip assembly has its limitations. Heat transfer from the chip takes place almost entirely through the bond pads. The bonds have small cross sectional area and some 400 are required in order to extract 1 watt of power from a chip with a reasonable temperature rise across the bond. High power and flip-chip assembly invoke active cooling in some form.

4. MCM CONSTRUCTION

MCM construction only introduces two novel features : large area substrate-to-package attachment and the interconnect fabrication.
The attachment of the substrate to the package is usually by means of an adhesive. The key features of the attachment are its freedom from voids, its stability during subsequent processing and assembly, and its shear strength. The last two are largely decided by the choice of adhesive. Freedom from voids is essential to eliminate local mechanical and thermal stress concentrations. It is achieved by the attachment process, not by the attachment material.

The interconnect wiring is deposited as a multi-layer structure on the silicon wafer surface. It is built up using well established methods of metal and insulator deposition combined with photo-lithography.

The processes used are adaptations of processes used in integrated circuit (IC) manufacture. They diverge from standard IC practice in the use of greater line widths, greater metal thicknesses, a wider range of metal types and thicker dielectric layers than in conventional integrated circuits.

An insulation layer thickness between 6 or 12 microns is required for transmission line structures with characteristic impedances of around 50 ohms. Thinner dielectric layers can be used where transmission line behaviour is not required.

The insulator material may be an organic compound such as polyimide, or an inorganic material such as silicon dioxide. Silicon dioxide has many attractions, not least the extensive background in IC manufacture, but it is difficult to obtain thick layers of it.

For this reason, most work has been devoted to polyimide or other organic insulators.

Different metals are used for different purposes.

Aluminium is easy to handle and has no compatibility problem with the chip metallisation. Copper is used for high current/low resistance tracks and other materials may be used for specific purposes.
Flip-chip assembly methods use multiple dissimilar metal coats between the aluminium interconnect on the chips and the solder used to connect chip to substrate.

Substracte manufacture is complex but does not break any radically new ground. The particular processes used with active substrates must be compatible with any temperature limitations imposed by the pre-diffused active devices.

5. SELECTING AN APPLICATION FOR MCMs

Any collection of interconnected chips can be assembled in the form of an MCM. The best applications for MCMs are those with high chip to chip connectivity but a low number of connections to other associated circuitry. This maximised the reduction in package pin count.
Connectiosn between the MCM substrate and the package pin are via wire bonds connected to bond pads at the substrate periphery. The substrate area required to accommodate the chips should be reasonably well matched the substrate periphery required to accommodate the bond pads. It is better if the dominant effect derives from the substrate area.

The total dissipation of the components and the range of individual chip dissipations must be consistent with the thermal properties of the substrate material, the adhesives between substrate and chip and between substrate and package, with the package and with the thermal path from package to final heat sink.

Packages suitable for MCMs are being developed. The size of available packages or the number of pins available may form a hard limit on module complexity. The limit may be hit with a few large chips or with a higher number of smaller ones.

There will always be some yield loss in assembly, on test of after burn-in. This yield loss will rise dramatically with chip count. MCMs with excessive chip counts become uneconomic. Testing can also be uneconomically expensive unless the module is readily testable as a stand-alone function.

Good candidates for MCM applications are relatively self-contained sub-systems with modest total power dissipation and no major "hot spots".

An example is the MIL STD 1553 Remote Terminal and Bus Controller MCM shown in Fig. 8. This hybrid executes the functions shown in Fig. 9 with the interfaces shown in Fig. 10. It has 12 chips - two analogue bipolar, four TTL, 2 SRAMS and 4 CMOS ASICs.

Figure 8

Figure 9

Figure 10

6. DESIGN AND MANUFACTURE AND TEST OF MCMs

6.1. Design

Fig. 11 shows the design flow involved in generating a silicon hybrid MCM. The sequence is not unlike that for designing an ASIC. It starts with a description of the hardware required and ends with geometric layout data for the substrate and the process instructions for assembly. Some elements of it are more like pcb design. The substrate layout problem shares many features with multi-layer pcb or multi-layer thick film hybrid layout. Yet it is the same as neither.

One difference appears in the design verification functions. Pcb design verification is usually confined to validating the interconnect net list and the observance of geometric design rules.

ASIC design verification also checks the observance of electrical rules. MCM design verification will frequently require checks on the observance of thermal rules.

A significant element in the thermal equation is the path between package and the ultimate heat sink. Neither ASIC nor pcb designs are influenced in this way by factors outside the particular component being designed. It is safe to design the ASIC without reference to how it is integrated into the system in whih it will be used.

This type of interaction is not confined to thermal analysis. Substrate design, as Fig. 11 shows, interacts with almost every other design activity except the design of the system. It will not be uncommon for the initial selection of a package to be rejected at the substrate design stage. The effect of this rejection will ripple through the design sequence back to the next substrate design iteration.

Figure 11

Design systems suitable for MCMs are starting to appear but will be extended and improved over the next year or two.

Existing MCM design systems are adaptations of pcb or C-type hybrid design systems. D-type MCM design will require extensions in several respects. Resolution usually needs to be improved. Variable line width must be provided (Fig. 8) as most pcb's and hybrids use a single line width throughout. Several of the major CAS suppliers (e.g. Valid, Logic, Cadence and Intergraph) are working on software specifically for MCMs and which will include the essentially new features such as thermal analyses, multiple pad rings and transmission lines. They will also need to provide for capacitors and resistors either deposited or diffused in the substrate. Active substrate design will require a full IC design package well.

The design of a silicon substrate is not the same as designing a pcb or a ceramic thick film substrate. It will usually be more complex than either and will demand more engineering knowledge.

6.2. Manufacture

Manufacture of the substrates is, in IC terms, not a difficult task. The physical dimensions are large compared with ICs ; the accuracy and cleanliness required are undemanding. The main complications arise where thick insulators are demanded or very good planarity over thick metal tracks. These are significant cost drivers.

Chip attachment and wire bonding are well established processes for the face-up chip assemblies.

Special equipment is required for substrate to package attachment and for flip-chip assembly. The precision with which the flip-chips have to be positioned on the substrate is at the limit of capability of standard pick and place machines but improved equipment is becoming available and very few flip-chip processes are qualified at present.

TAB assembly methods are being investigated. They are particularaly attractive for automatic high volume assembly.

6.3. Testing

Testing is involved at many stages in the manufacture of an MCM. Parametric tests are used to validate the process steps in substrate fabrication.

Wafers which pass parametric screening are tested to ensure correct connectivity on all conductor tracks. The chips to be mounted on the substrate are tested on the wafer in a procedure similar in principle to that used for substrates. However, the tests must be severe enough to reduce the incidence of chip failure or of performance deficiencies after assembly. Rework on MCMs is usually difficult even with reflow-soldered flip-chip assembly.

In order to reduce the impact of this type of failure the substrate may be tested when partially or fully assembled. The choice will depend upon rework possibilities, the rate at which value is added and the yield which can be expected. Military and other specialised product requires testing at temperature extremes before and after burn-in. Various centres are working on procedures for die burn-in before wafers are sawn.

The test methods and test programs to be used for substrate testing must be established as part of the design process. The principles and procedures are similar to those adopted for IC design and test. Test vectors are prepared in the format appropriate to the test equipment to be used. These vectors are then applied to the simulated interconnect pattern and analysed for fault coverage.

Various types of substrate tester are in use or in development. Two methods are in current use. One uses a two point prober to check for continuity of the metal tracks and intermetal layer vias. The other uses capacitance techniques and detects the change of capacitance where open circuits shorten a track or short circuits increase it. One strategy uses the capacitance method to identify problem areas which are subsequently explored by a two point prober.

Probing the substrate is clearly undesirable and non-contacting methods are being explored. The use of active substrate techniques has also been proposed but its economics are not established. There is likely to be more progress needed in substrate testing than in any other area. Speed of testing and wafer damage by testing are two critical issues. There are other test operations required. Chips need to be tested before use in the MCM and the module needs to be functionally tested after assembly. These are handled, using normal methods, by the chip supplier, the MCM supplier or the final customer as is most appropriate.

7. RELIABILITY

There are two ways of comparing reliability. One is by comparing statistically significant in-service data. The second is analytical and uses standard data e.g. taken from MIL HANDBOOK 217. Clearly, the first method is impractical in the absence of extensive in-service experience. The second is difficult because it requires interpretation of data gathered from C-type hybrids and from discrete integrated circuits.

The MCM shown in Fig. 8 is packaged in a 100 lead PGA with a modified well. It therefore seems reasonable to take package reliability data directly from the handbook. The chip data can also be extracted directly from tables in the handbook. A typical substrate has a net count equivalent to a 250 to 300 gate array but contains no active elements.

A figure for the substrate reliability can be obtained by increasing the reliability figure for a 300 gate array to allow for the absence of active circuits and also to allow for the much greater line widths and line spacing used in the MCM interconnect. With this data, and under defined environmental and installation conditions, it is possible to calculate a reliability figure which will be consistent with data for other devices obtained using the handbook procedures.

A comparative analysis has been conducted for the function shown in Fig. 8. The MCM failure rate was calculated as described above. The same function was then analysed for a C-type hybrid in an appropriate package. finally, the same calculation was carried out for discrete components on a pcb. The analysis started from the points on the circuit board corresponding to the pins on the PGA package. It includes all the soldered joints and wiring within the confines of these pins.

The results were obtained for the following conditions :

PGA package
Total dissipation 1.5 W
Equipment installed in the inhabited zone of a fighter aircraft
Package temperature 90°C
MIL STD 883 level B-1 release

Version	Failure rate/million hours
D-type MCM	1.4
Discrete Parts	3.2
C-type hybrid	8.0

A similar analysis was applied to a function comprising a micro-processor and 1, 2 or 4 DRAM chips. The analysis compared discrete parts and a D-type MCM version.

The results obtained for the following conditions :

PGA package
Total dissipation (1 + 0.5/DRAM) watts
Rotary wing vehicle
MIL STD 883 level B-1 Release
are :

	Failure /million hours		
No. DRAMS	1	2	4
Silicon MCM	3.247	3.947	5.367
Discrete ICs	3.05	3.921	5.665

8. ACQUIRING A D-TYPE MCM

Acquiring an MCM has much in common with procuring an ASIC so far as the design entry points are concerned.

However, there are two possible ways of handling the assembly and the testing of the hybrids themselves.

As with an ASIC, customers can enter their requirements at three points in the design cycle. The first is as a specification in a turnkey approach. It if highly desirable that a hardware description language such as VHDL or ELLA be used to express the required specification. The manufacturer will prescribe the particular dialect to be used. He will be responsible for all aspects of the design from this stage.

The second entry point is at simulated netlist, supplied with the test vectors used. The use of customer generated test vectors is essential to keep the customer/vendor interface clearcut. The customer will need to have access to approved design CAD to carry out this activity and will be required to supply the netlist in specific format. Even at this stage he may also be required to supply additional data.

The call for this data depends upon who procures the chips to be used in the MCM. Many vendors will prefer customers to supply free-issue chip-kits. This approach gives the customer direct control over his timescales. The vendor will hold the customer responsible for the supply and accuracy of the geometric data and pad allocations for the chips to be used. The customer will also be required to define the package style to be employed and any pin-out preferences. No substrate design activity can commence until all of this data is complete and a net list is submitted in approved format.

From this point the vendor will proceed to "place" the chips on a substrate, route the interconnect and position the contact pads. At this stage tow cross checks are made besides the standard layout versus schematic (LVS), design rule checks (DRCs) and post layout simulations. First, whether the substrate will fit in the well size of the standard version of the preferred type of package. Second, a thermak analysis to expose any temperature problems, locally or generally. Any problems exposed by these checks will require changes to the customer requirement e.g. change of package size and pin allocation or the addition of cooling structures.

This process will iterate until customer and vendor have agreed on all aspects of the physical design.

The third entry point is at layout. It is arrived at by the customer himself following exactly the same sequence as described above. It culminates in the submission of geometric layout data in some standard format such as Calma GDSII or CIF. Most vendors will only accept layout data from a few well qualified and vendor-approved sources.

Prototypes will be made from this data and supplied for customer approval prior to production release. Some customers, particularaly those who have completed their own layout, may wish to procure unpopulated by tested substrates to assemble themselves. However, most users will wish to purchase complete hybrids.

Two forms of production part are likely to be offered. In the first, typical of turnkey projects, the vendor supplies fully tested parts

using test vectors supplied by the customer. In the second approach the vendor will supply a customer with assembled but untested parts. The vendor/customer interface to possess or have access to appropriate ATE. Many vendors will promote the free-issue chipset and untested part combination because it limits their risks and enables them to price their work with greater confidence. However, many customers will not be equipped either materially or skill-wise to follow this route.

Choice of package is a variable which may affect some procurements. Substrates are fabricated, like ICs, on a circular silicon wafer of 4, 6 or 8 inch diameter. For each wafer size there is a series of integer numbers of substrates of sizes which just fill the wafer (Fig. 12). Vendors are likely to tool a selection of packages with wells which accept these substrate sizes. Non-standard packages will incur tooling charges and, very often, significant stretch in timescales.

As noted earlier, MCM design and procurement has features common with ASICs and the C-type hybrids but involves additional complexities not found in either of the other products.

Figure 12

9. SECONDARY EFFECTS

MCMs will lead to design innovations which are not related to the features which spurred their development. For instance, flip-chip assembly removes the existing restraints on chip pad count. Chip-set architects will be able to use data and control highways of unlimited width, with overall benefit to system performance.

The power densities found in many MCM designs will spur the introduction of new package structures and materials. Examples are aluminium nitride (with high thermal conductivity, and a TEC matching silicon) or metal reinforced plastic in which expansion coefficients can be tailored to requirements. Improvements will be demanded not only in the thermal management of the packages but in the design of the thermal paths between the package and the ultimate heat sink. At this stage it may become necessary to couple the design of the MCM with the enclosure in which it tis mounted. No doubt there will be other unforeseen effects as applications broaden.

Chip failure rates, between functional test prior to assembly and post burn-in test, currently limit the complexity of the hybrids which can economically be assembled. Redundancy techniques, preferential wiring and wafer burn-in could be used to offset this difficulty and to permit more complex MCMs to be constructed than is presently possible.

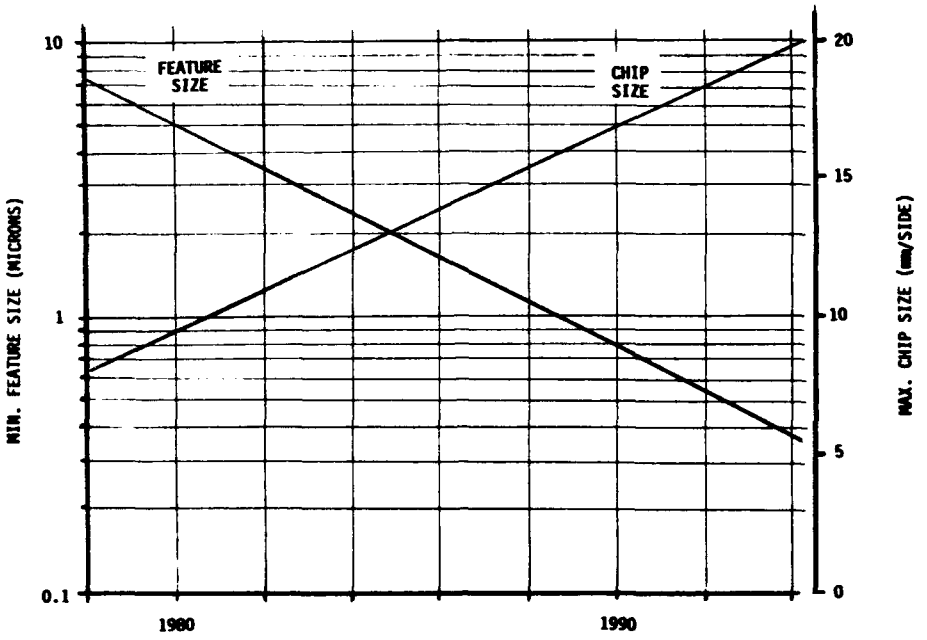

FIG.1 FEATURE SIZE & CHIP SIZE (CMOS) VS. TIME

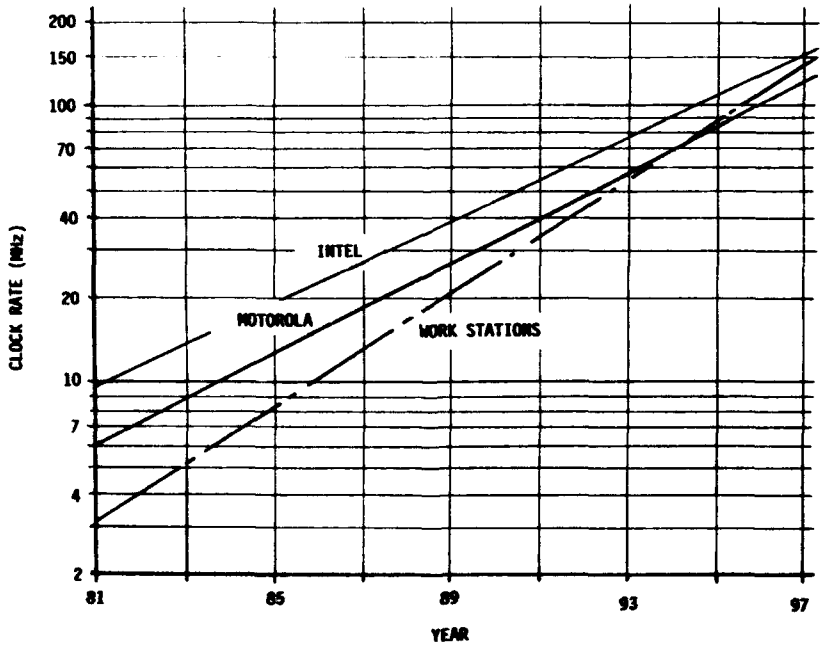

FIG.2 MICROPROCESSOR CLOCK RATES

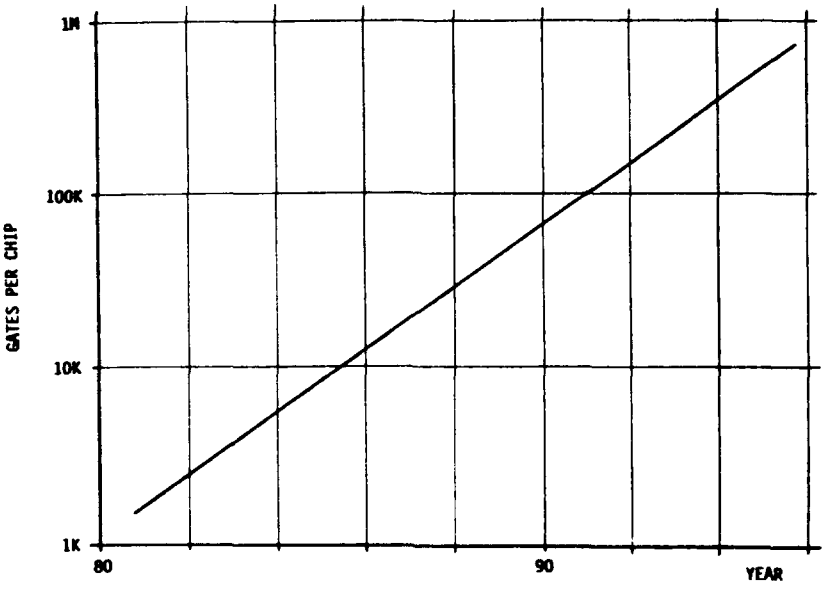

FIG.3 CMOS COMPLEXITY VS. TIME

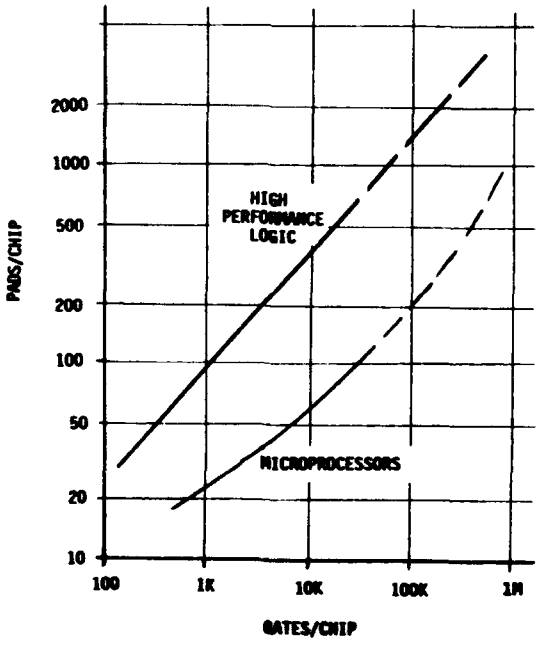

FIG.4 RENT'S RULE

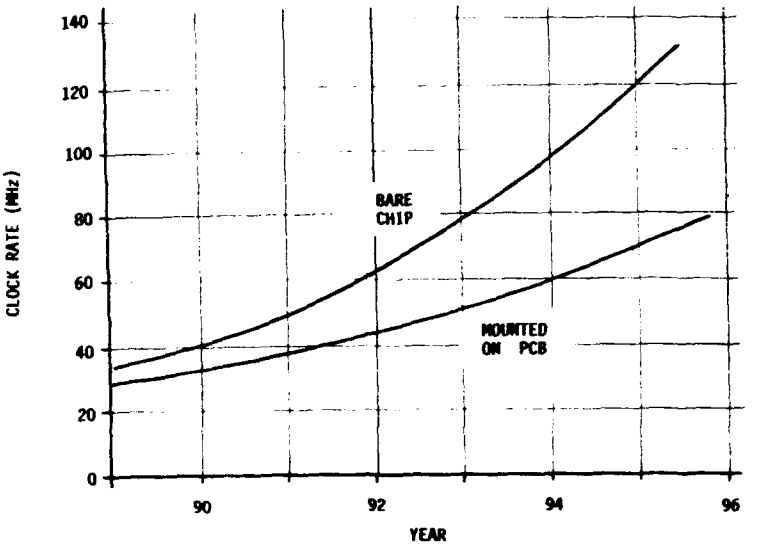

FIG.5 BARE CHIP VS ON BOARD SPEEDS

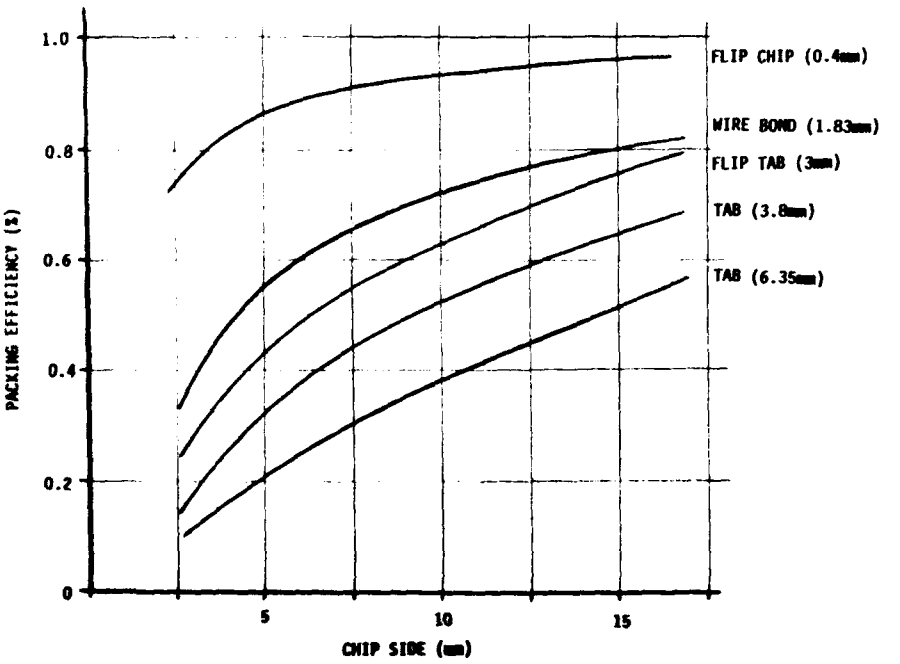

FIG.6 THEORETICAL PACKING EFFICIENCY

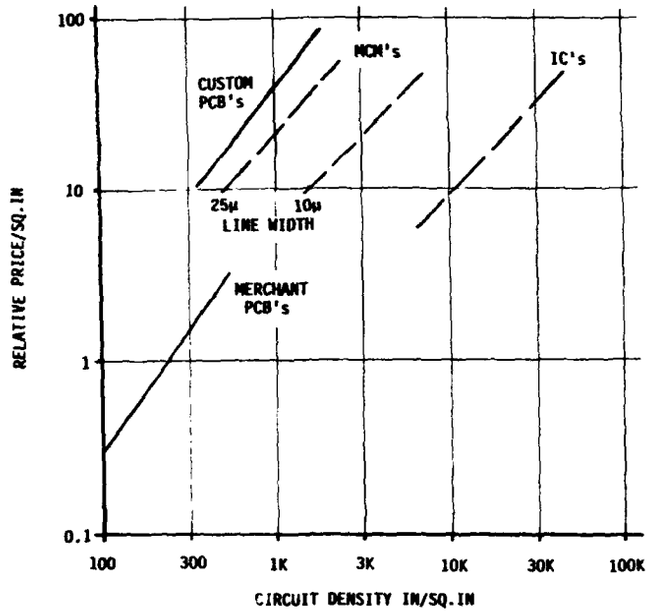

FIG.7 COST COMPARISONS

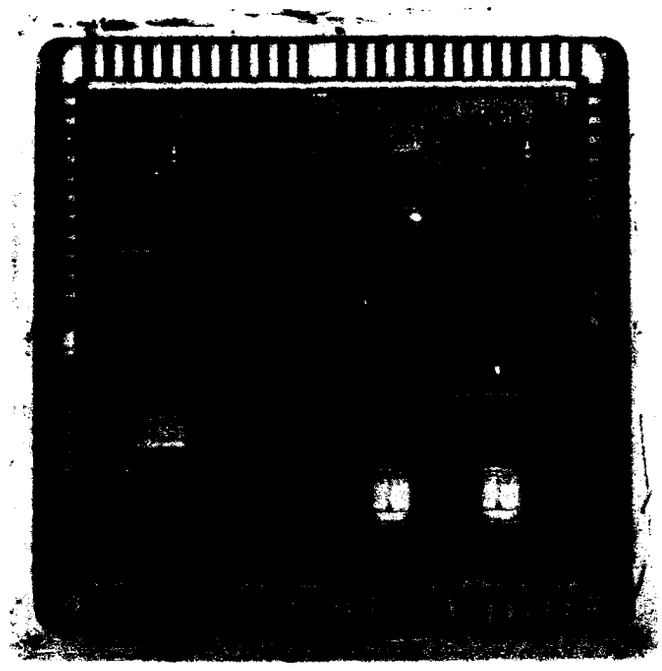

FIG.8 DUAL RT/BC/MME-MULTIBUS INTERFACE

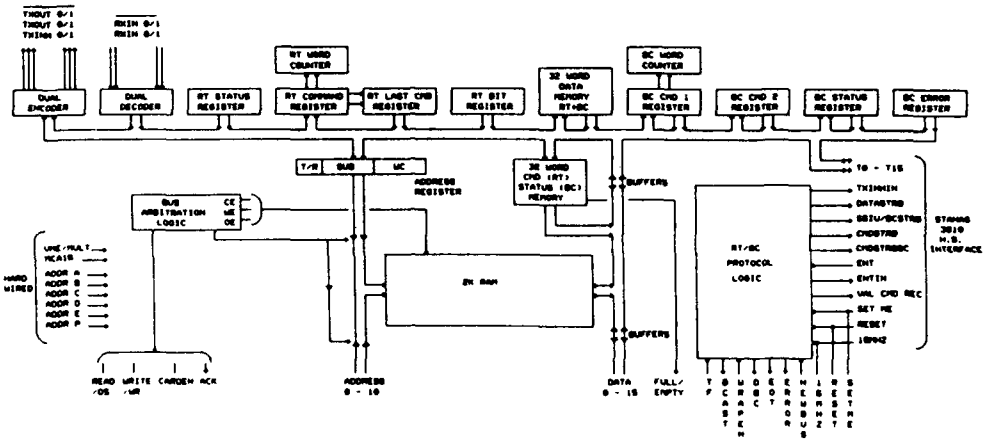

FIG.9 BCU/RTU FUNCTIONAL DIAGRAM

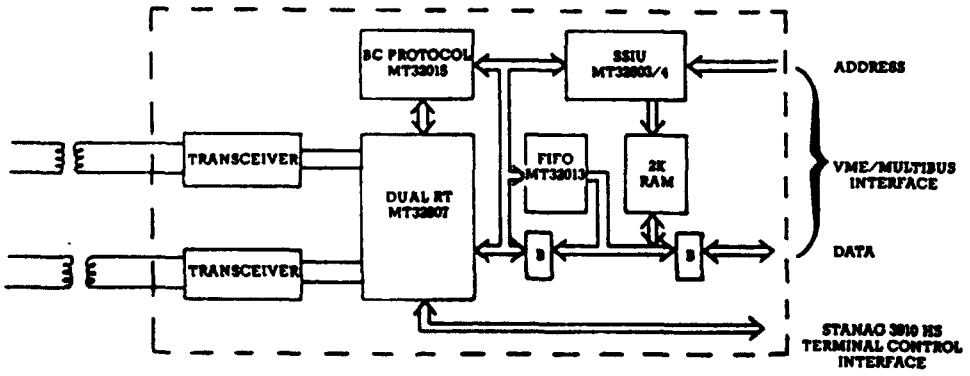

FIG.10 DUAL RT/BC/VME-MULTIBUS INTERFACE

Design Flow for systems built on Silicon Hybrids

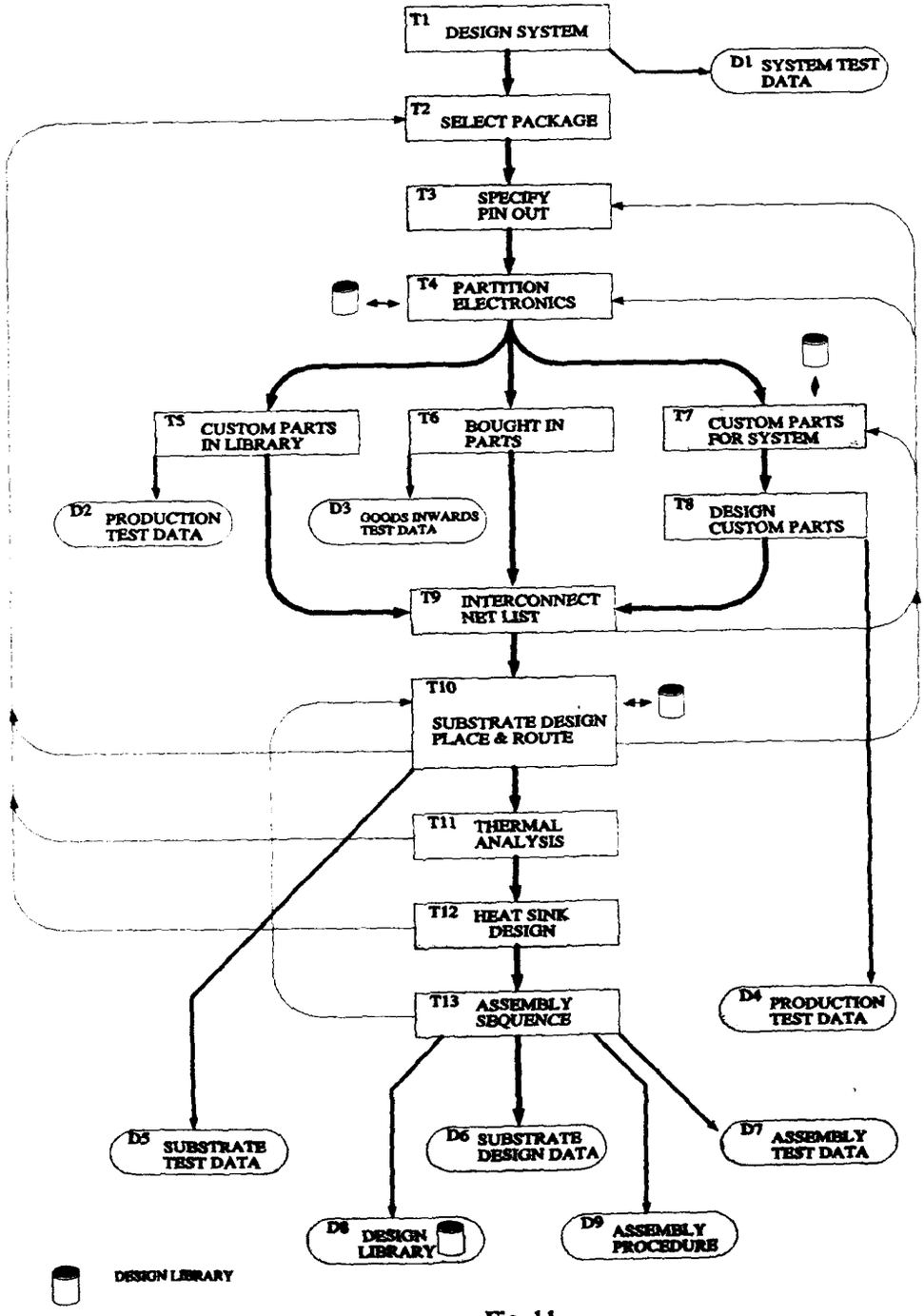

Fig. 11

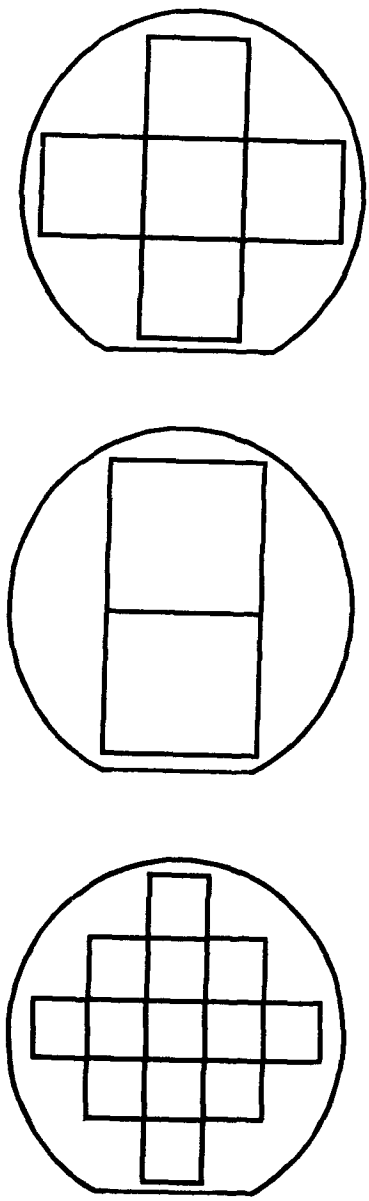

FIG.12 CHOICE OF SUBSTRATE SIZE

A RADAR SIGNAL PROCESSING ASIC AND A VME INTERFACE CIRCUIT

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80 avenue P. Brossolette, 92120 MONTROUGE, FRANCE

ASIC # 1 : SIGNAL PROCESSING

1. APPLICATION

The purpose of this circuit is to perform real time signal processing for radar applications such as missile seeker.

The signal input is a succession of "frames" = 5 blocs of 512 words, on which the following functions are sequencially performed :

- Input sampling
- Pre-processing (speed and acceleration compensation, weighting...)
- Spectral analysis (DFT, with calibration)
- Side Lobe Cancelation
- Power of signal
- Detection
- Post-processing

There are 2 operating modes (standard and samples accumulation) and a variety of options through user selectable parameters and control logic (i.e. detection with global, local or fixed threshold).

2. MAIN CHARACTERISTICS OF THE ASIC

Architecture :
- I/O interfaces with ROM, EEPROM (coefficients), slave SRAM (data storage)
- # 16 bits data bus
  2x (128x16) internal memory
- Internal/external address generation
- Operative part → filter, multiplier, adder
- Control logic

Physical :
- 1.0 µm, dual metal layer, CMOS technology
- 65K used gates on a 100 K "sea of gates" array (LCA 100K)
- 2.25 sqcm
- 223 pin PGA package
- 1 W power dissipation

Performance (over mil. temp.) :
- > 20 MHz system clock
- Throughput 5x512 samples/10 ms
- 1 cycle (10 ms) latency
- FFT = 5 Mega-butterfly/s
- Overall performance : 36 Mops

3. DESIGN CYCLE

Hardware platform : SUN3.

Software tools : ASIC vendor tools (LSI logic MDE) + Verilog (for simulation).

Starting from the original specification (list of the algorithms to perform), the whole design took 2 persons during one year.

The ASIC development cycle was as following :

Internally :
6 months :
- Behavioral modeling.

3 months :
- schematic capture
- use of generators for RAM blocs ("soft megacell")
- logic simulation
- pre-placement (floorplanning)
- timing and critical path analysis

Supplyer :
3 months :
- place and route, verify
- fab of masks and prototypes

Results :
The device was delivered in time, and first time full spec operating.

Besides that, for full function validation and fast prototyping a first generation circuitry, with limited functionality, was designed with discrete components. It uses a standard DSP (320C30) and programmable logic.

4. INTEREST OF THE ASIC APPROACH

Compared with the discrete component solution, the ASIC enabled us a substantial increase in

performance (nb of Mops multiplied by 7) and reduction in board area :

	#1 discrete components	#2 ASIC
Nb of ICs	1*TMS320C30 (PGA 180 pin) +4*PROM 64K + 1*EPMAX 68 pin	1*PGA 223 pin
Relative fonctionnality Nb of ops performed	1	2.5
Computing time (FFT 256 pts)	1.5 ms	0.5 ms

Power dissipation and purchasing cost have also been reduced by a factor > 2.

Figure 1

Figure 2

ASIC # 2 : EDVIGE

1. APPLICATION

Monochip solution for VME interface, 68xxx compatible.

2. MAIN CHARACTERISTICS OF THE ASIC

Features :

- VME interface controler and arbitration
- Full buffering of local and VME bus signals
- Direct connection to 68xxx microprocessors
- Master/slave operating mode
- Interrupt controler (interrupt stack, internal timer)
- Programmable Watch-dog
- Data transfert through 42 Mbits/s DMA
- 32 MHz clock

Technology :

- 1.5 µm BICMOS (for high output drive)
- 20K used gates on a 35K gate array (LDD10035)
- 72 mA output drive
- 299 pins PGA package
- 4 W max dissipation

3. DESIGN FLOW

The ASIC vendors dedicated tools were used, on a SUN 3/60 platform.

As the function already existed and had been validated with discrete components, no high level modeling was made.

The design started at the netlist level. Logic simulation with toogle test was performed.

Results :

The design turned out to be much more complex than estimated, with critical problems of a very large "glue logic" blocks interfacing 2 completly asynchronous worlds.

Nethertheless, first Silicon was operating at full speed, with one functionnal bug due to the design. A new mask set will be realized.

4. INTEREST OF THE ASIC APPROACH

This monochip solution replaces a whole circuitry with approx. 12 devices in a standard design. This means a dramatic reduction in :

- board area
- power consumption
- design complexity

There are also indirect advantages in term of MTBF and cost of the test of the function.

Nota : the circuit will be commercially available as "standard chip".

Annex : EDVIGE features

ENVIRONNEMENT

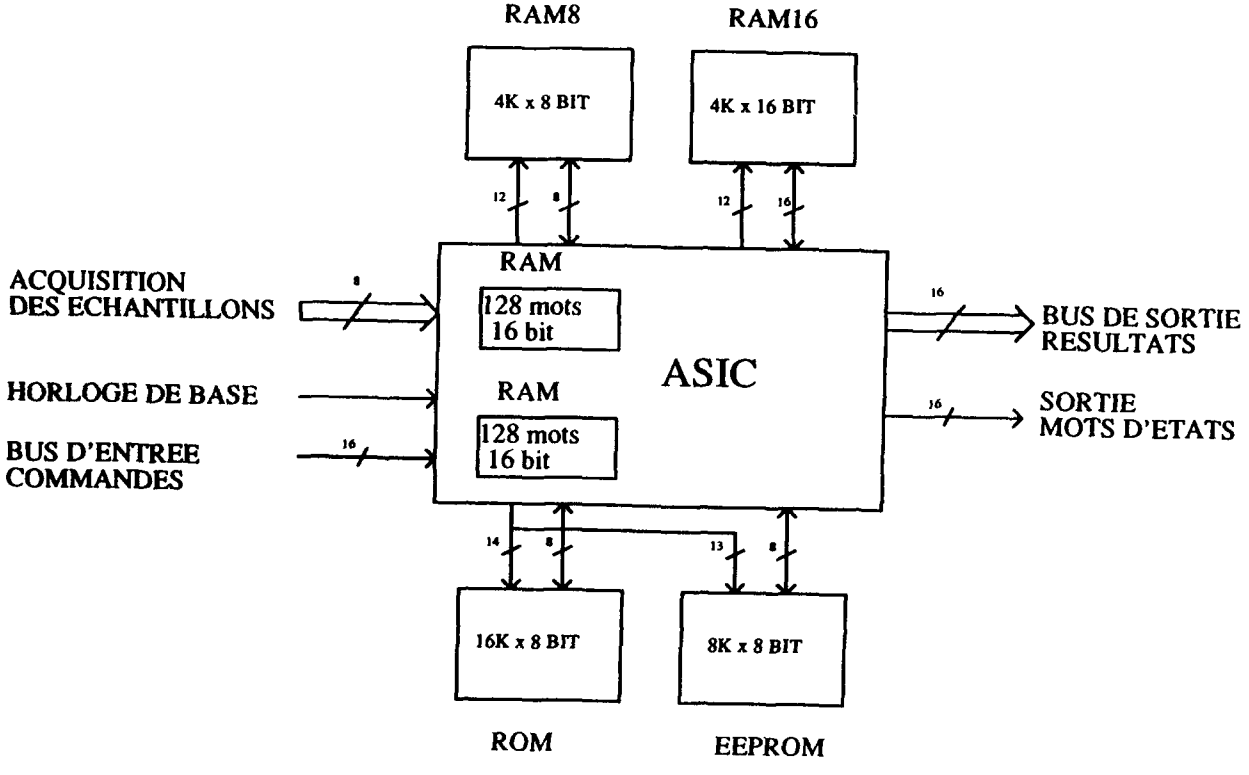


Figure 1

ARCHITECTURE

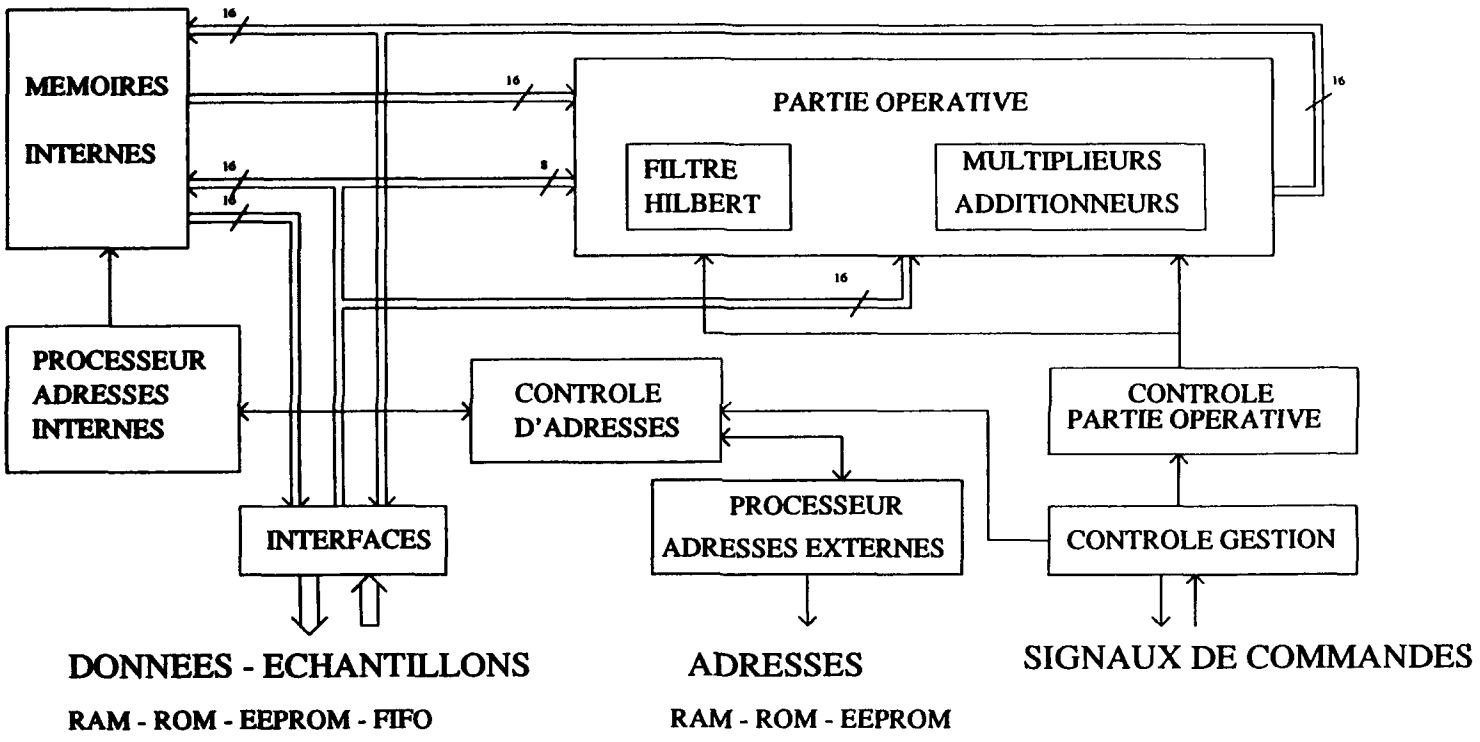
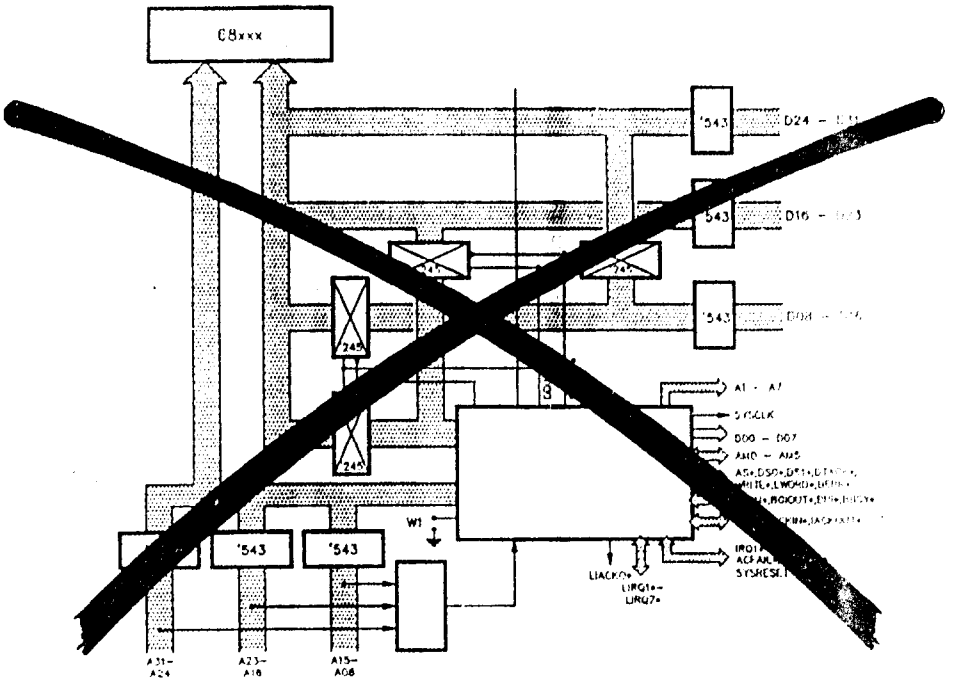


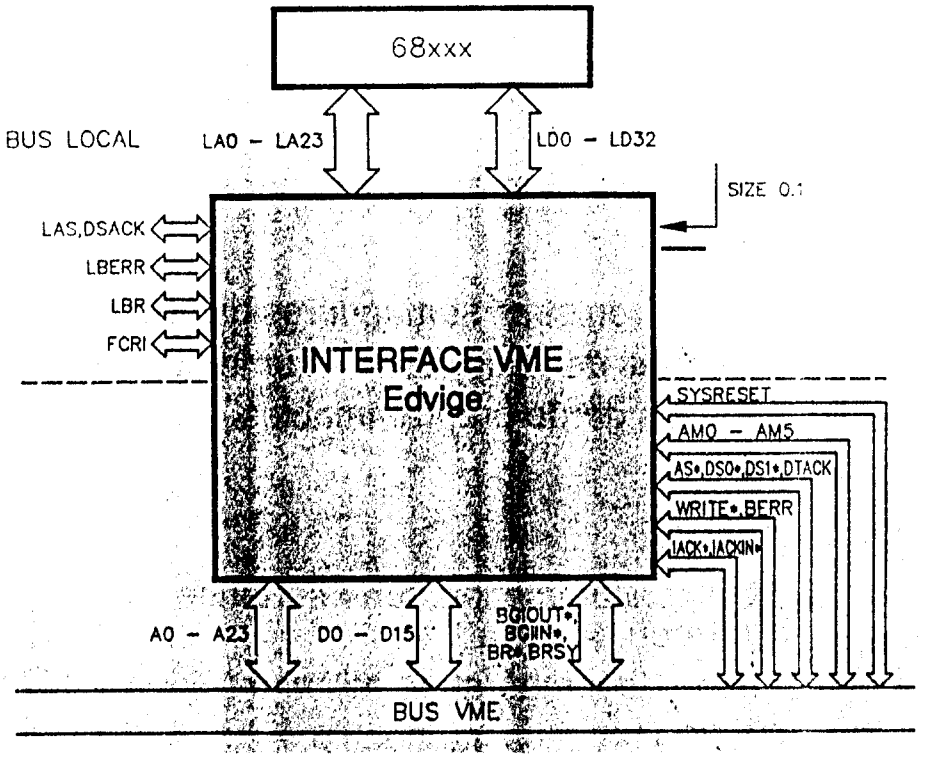
Figure 2

ANNEX

HALTE AUX SCHEMAS COMPLIQUES



NOUVEAU SCHEMA PROPOSE



ANNEX

CARACTERISTIQUES

- **CONTROLEUR INTERFACE VME ET ARBITRE**
  - Configuration et contrôle par programmation de 32 registres.
  - Bufférisation complète des signaux VME et contrôle (adresses et données).
  - Bufférisation complète des signaux du bus local et contrôle (adresses et données).
  - Connexion directe aux microprocesseurs de la famille 68 XXX.
- **FONCTIONNEMENT MAITRE/ESCLAVE**
  - Ecriture, lecture.
  - Affectation dynamique des adresses locales vues du bus VME.
- **TRANSFERT DE BLOCS DE DONNEES**
  - Assuré par DMA (42 M bits/s).
- **ARBITRAGE**
  - SGL, PRI, RRS.
- **INTERRUPTION**
  - Timer interne.
  - Empilage de 16 interruptions par appel.
- **DIVERS**
  - Plusieurs registres sémaphores disponibles.
  - Possibilités de "daisy-chain" sur le bus local.
  - Chiens de garde programmables.
- **TECHNOLOGIE**
  - BICMOS
  - Faible consommation, forte sortance (48 mA ou 64 mA).
  - Gamme de température militaire (-55° à + 125°).
  - PGA 299 broches, monochip.

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Signal processing	Display devices

14. Abstract

This document presents an overview of how ASICs are a key factor in the future of avionics systems. The technical capabilities and possibilities of ASICs in avionics applications are discussed along with essential characteristics and various types of ASICs that are available.

The CAD tools necessary for the rapid development of these integrated circuits are discussed. Two specific examples of applications are cited including the imbedded computers necessary for airborne radar digital signal processing and the ASIC role in image processing for aircraft cockpits.

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